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S32G-VNP-RDB2

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Drawn by: Helen Xu	Page Title: TITLE PAGE		
Approved: Tao Xue	Size C	Document Number SCH-47440 PDF: SPF-47440	Rev D3
Date: Tuesday, March 16, 2022		Sheet 1 of 33	

Revision History

Revision	Date	Description
X1	Jun 30, 2020	Rev X1 Draft
C	Jul 28, 2020	Final Release
C1	Sep 10, 2020	1. DNP R1190, U125, U126, R1184, R1150, populate R1191, R1185, R281 to disable F80B control on the board 2. DNP C1888, C71, C91, C89, C90, C137, C138, C158, C155, C202, C191, C231, C233, C1678 to reduce VRS510 LDO3 ramp up time 3. DNP C10 4. DNP R367, R735, populate R437, R690 to change U58 PHY Address to 0x04 5. DNP R1203 6. Populate R951, R1204 7. Change C1676 and C1677 from 22uF to 1uF 8. DNP L519
C2	Nov 4, 2020	1. Replace SW1 & SW2 with short actuator part 2. Replace all TJA1043ATK with TJA1043TK 3. Change U41 from PVR5510AMDA4ES to PVR5510AMDAHES
CX1	Jan 9, 2021	1. Update U92 PF5300 to latest symbol and footprint, add test point on FB+ 2. Update U94 from PF5500AMMA4ES to PF5500AMMA7ES and change L520, L521, R957, C1787, C1788 value accordingly 3. Add U41 VRS510 separated BUCK1 and BUCK2 output option for S32 G3, add test point on BUCK1_FB 4. Change U41 VRS510 VCOREMON & LV_HVLDQ_IN connection from near to S32 G 5. Add S32 G core current measurement circuit U136 and add to I2C4 6. Change U86 from AQR107-B0-EG-Y to AQR113C-B0-C 7. Change U106 PF5020AMBADES SW1/2 output 0.85V to SW1 output 0.7V, SW2 output 1.0V and SWND1 output 2.0V to support AQR113C 8. Change U89 from NX25V4006EM11-13G to AT45DB041E-S8HN2B-B to support AQR113C 9. Disconnect 100MHz LVDS_P100MHz_LVDS_N and add test point only, AQR113C doesn't need it 10. Add open Jumper J185 on VRS510_F80B and populate R1190, U125, U126, R1184, R1150 11. Change the power rail of U119 and U133 from +3V3 to P3_3V_I03P3 12. Add PL104 connection to enable FS9900 and load switches 13. Replace R43 with Jumper J186 14. Remove R224, R575 220hm from eMMC_CLK and SD_CLK, add 0ohm on uSDHC_CLK 15. Add 0ohm on DSP11_SOUT, DSP11_PCS0, DSP11_SCK and DSP11_SIN 16. Add 3-Pin header J186 on FLEX_LIN2 interface 17. Add Temperature Sensor U137 and add to I2C0 18. Change R416, R417, R336 and R337 from 10K to 1K 19. Replace obsolete U124 NX5P2924BUK with NX30P0121UK 20. Replace obsolete U135 NX5P2924BUK with NX3P1108 21. Connect R954 to the right side of R1077 22. Change U92 PF5300 FB connection from P0_8V to PMIC_SENSE 23. Change U92 PF5300 G1, G2, G3, G4 pins to 'NC' (floating) 24. Change L519 from 120nH to 100nH 25. Change R903, R402 from 10K to 20K, C1945, C1944 from 10uF to 1uF 26. Add pull-up, pull-down resistors on CLOCK_OUT0/ CLOCK_OUT1 and DNP. 27. Connect PF_PG000 to ADC_CH_08 as an option 28. Change R229 from 68.1K to 62K, R244 from 22K to 27K for board revision D
D	Jan 25, 2021	Final Release with CX1 update
D1	May 11, 2021	1. DNP TP106 2. Change R915 from 1.3K to 0ohm
D2	Nov 8, 2021	1. Update Power Tree and Reset Tree 2. Update SJA1110 Boot Option Table 3. Add pull up R1233 on AQR113C pin SIN 4. Change VDD_IO_SDHC and VDD_IO_GMA400 from P1_8V_IO to P1_8V_ANA 5. Update U43 to orderable part number S32G274AABN0VUC7 6. Update U41 to production part number MVR5510AMDAHES 7. Update U46 to orderable part number SJA1110AEL
D3	Mar 15, 2022	1. Change R1194 monitor voltage from PF53_0V8 to P0_8V 2. Change eMMC part U28 from MTF32GBALBH-AAT (not recommended for new design) to MTF32GAZAQHD-AAT 3. Change the 3-pin header to R1243 for U28 VCCQ 3.3V1.8V option, fix to 1.8V 4. Add U144 to have the logic control to support default voltage of VDD_IO_SDHC for eMMC is 1.8V, and for SD is 3.3V 5. Change U15~U18, U71~74 from TJA1043TKY (Not Recommended for New Design) to TJA1043TK/Y 6. Change U87, U111 from NT50102GD-Q100H (End of Life) to NT50102GT,115 7. Add resistor divider on PF_PG000 for ADC_CH_08 8. Populate TP106 9. Update U96 from PP5020AMBACES to SPF5020CMBACES (Production Part Number) 10. Update U108 from PP5020AMBADES to SPF5020CMBACES (Production Part Number)



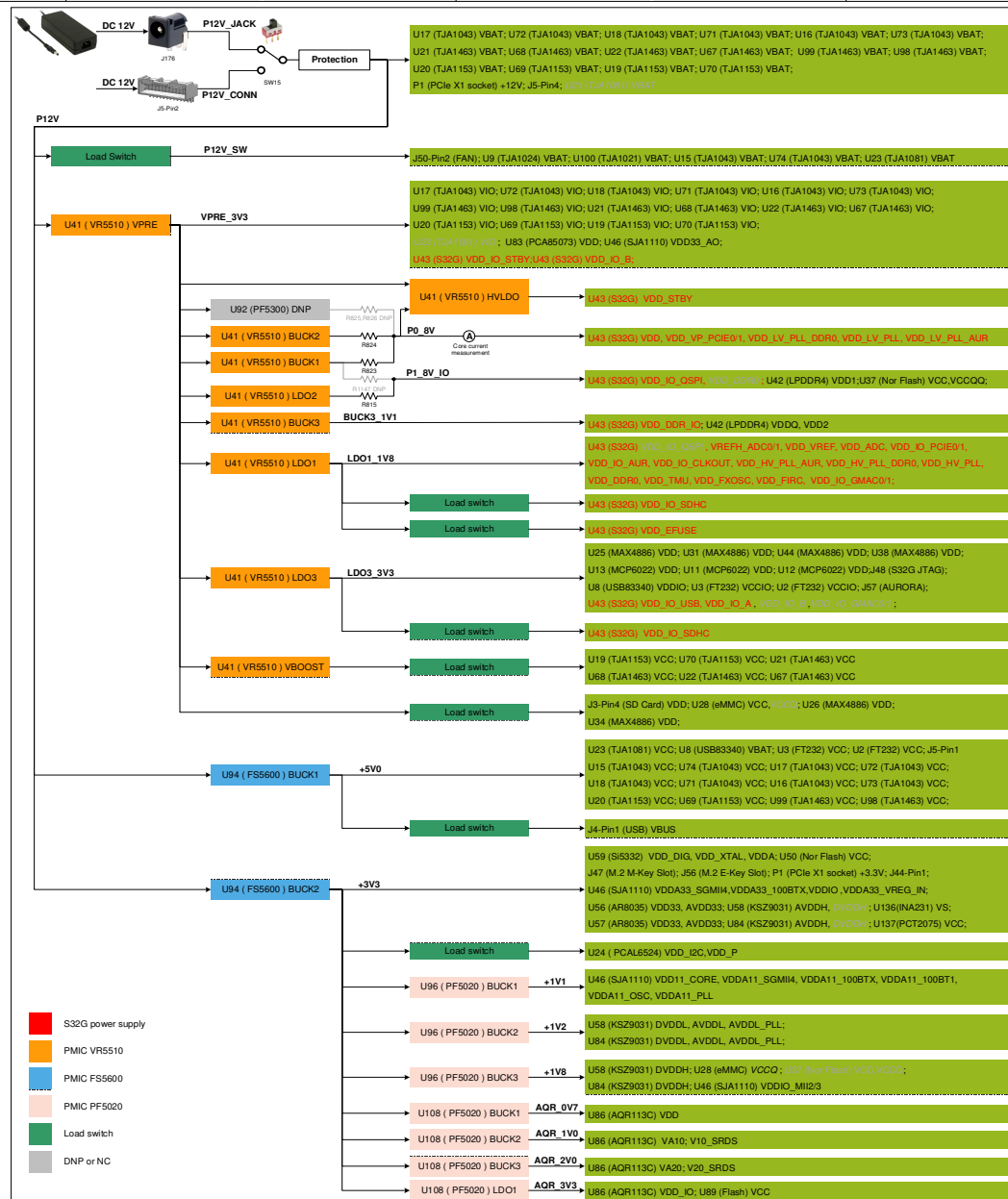
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Size C	Document Number SCH-47440 PDF: SPF-47440	Rev D3
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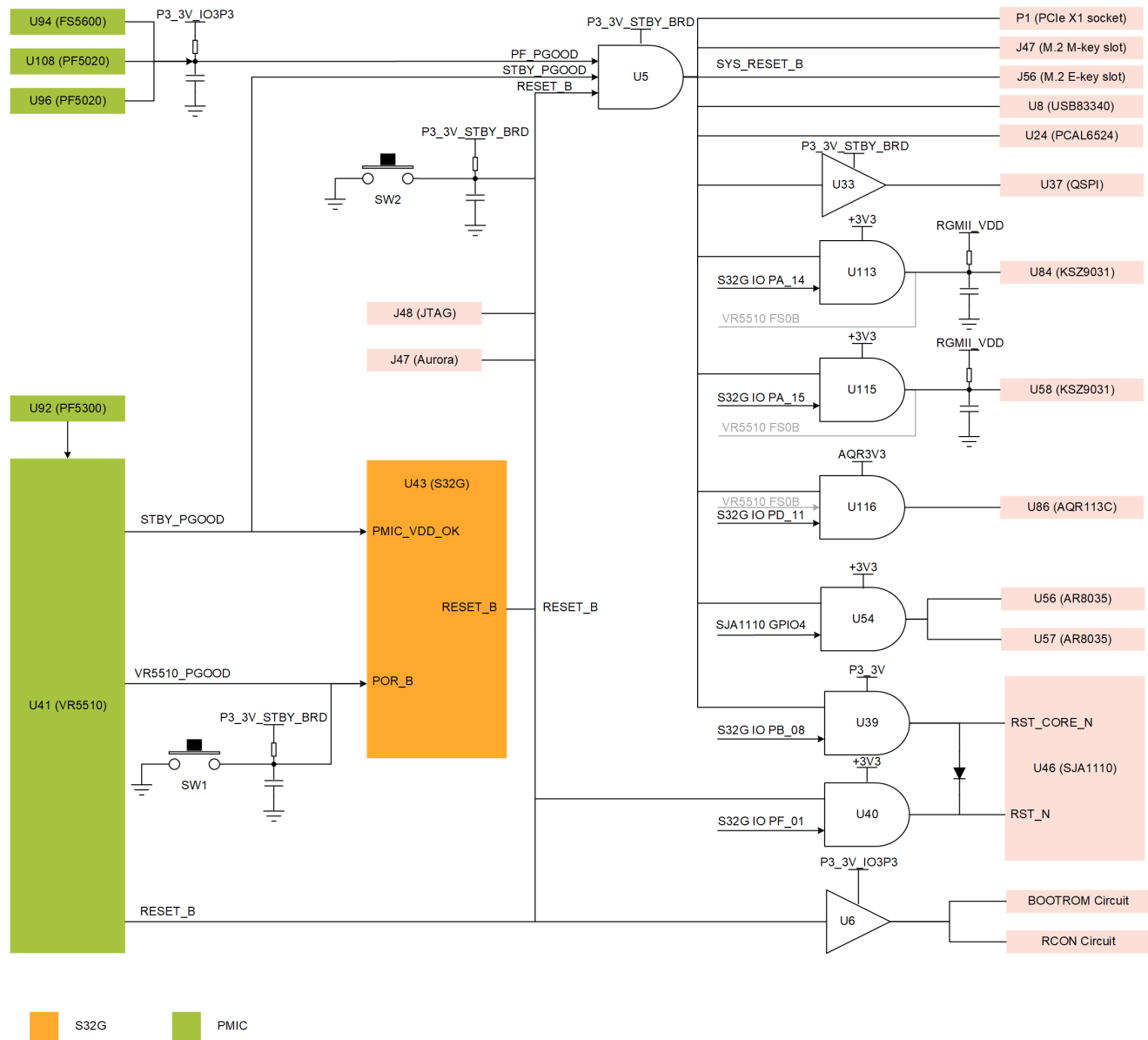
I2C ADDRESS

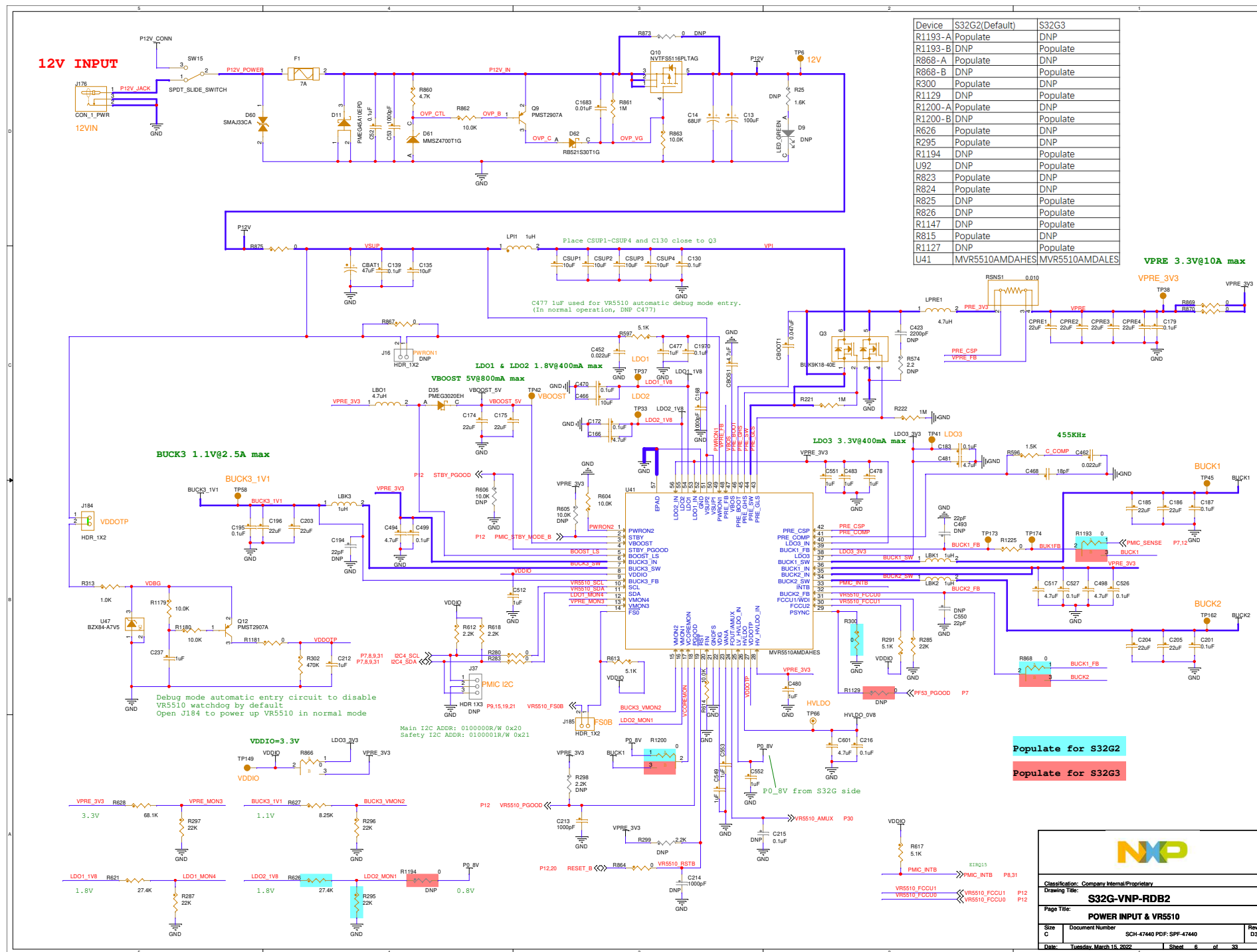
S32G Interface	Device	I2C Address	Description
I2C0_SCL PC_00 I2C0_SDA PB_15	U83	PCA85073A	1010001R/W 0x51
	U137	PCT2075	1001000R/W 0x48
	U59	Si5332	1101010R/W 0x6A
	P1	PCIe x1 socket	
	U24	PCAL6524HEAZ	0100010R/W 0x22
I2C4_SDA PC_01 I2C4_SCL PC_02	U41	VR5510	Main : 0100000R/W 0x20 Safety: 0100001R/W 0x21
	U94	PFS5600	0011000R/W 0x18
	U92	PF5300	0101000R/W 0x28
	U108	PF5020	0001000R/W 0x08
	U96	PF5020	0001001R/W 0x09
	U136	INA231	1000000R/W 0x40
I2C2_SCL PB_05 I2C2_SDA PB_06	J5	Connector	

ETHERNET PHY ADDRESS

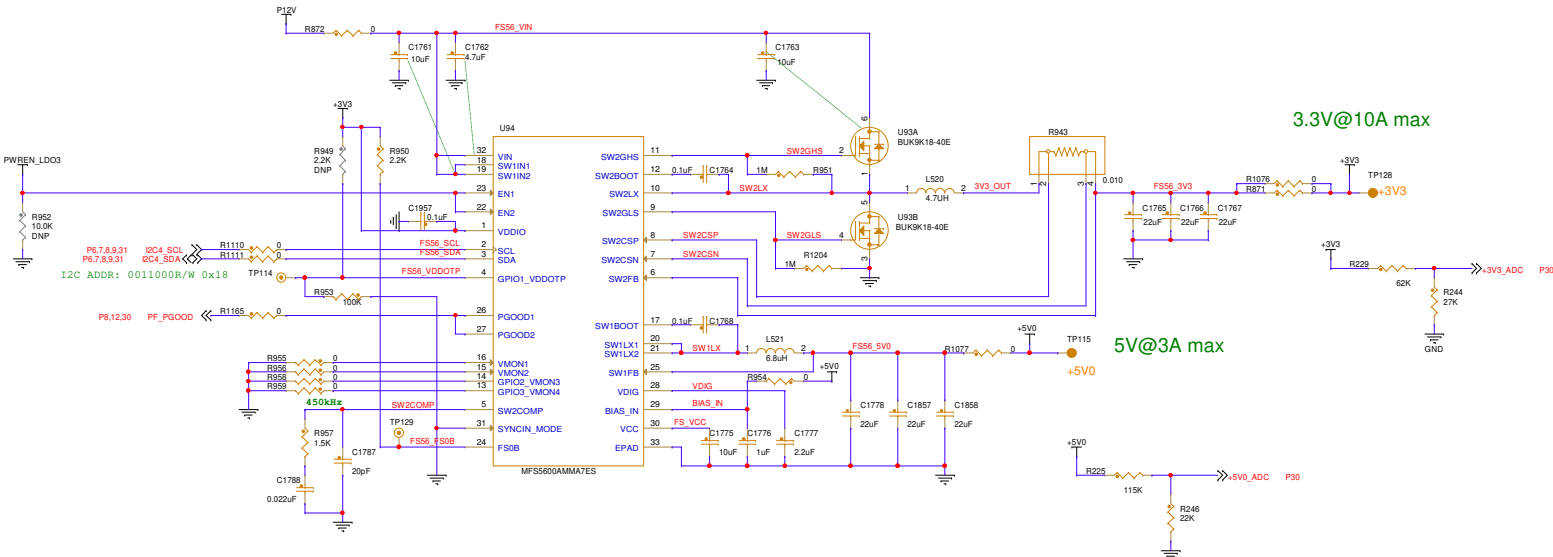
SMI Bus	Device	SMI Address
S32G PD_12(GMAC0_MDC/PFE_MAC1_MDC)	U84 KSZ9031	0X01
	U86 AQR113C	0X00 or 0X08(Default setting)
	U58 KSZ9031	0X04
S32G PE_15(PFE_MAC0_MDIO/PFE_MAC2_MDIO) PF_02(PFE_MAC0_MDC/PFE_MAC2_MDC)	U46 SJA1110	100BASE-T1 PHY1(Port5) 0X09 100BASE-T1 PHY2(Port6) 0X0A 100BASE-T1 PHY3(Port7) 0X0B 100BASE-T1 PHY4(Port8) 0X0C 100BASE-T1 PHY5(Port9) 0X0D 100BASE-T1 PHY6(Port10) 0X0E
SJA1110 SMI_OUT_MDC	U57 AR8035 U56 AR8035	0X04 0X05



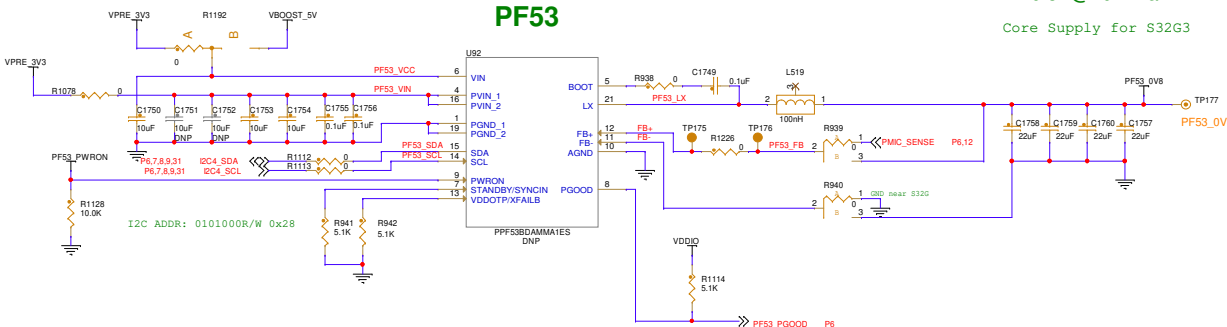




5V0/3V3 Power Supply



PF53

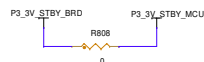
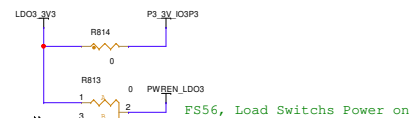
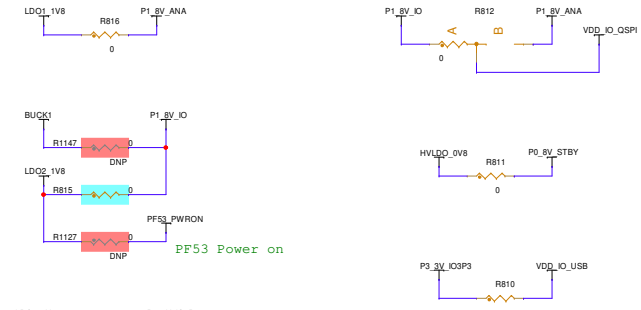
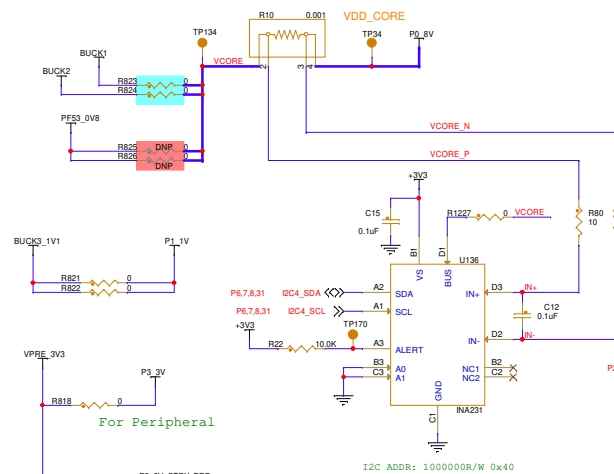
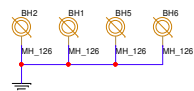
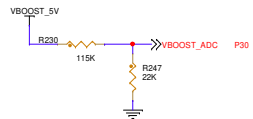
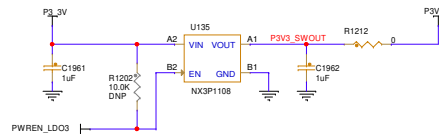
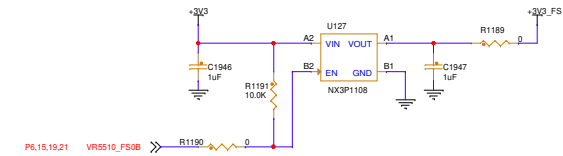
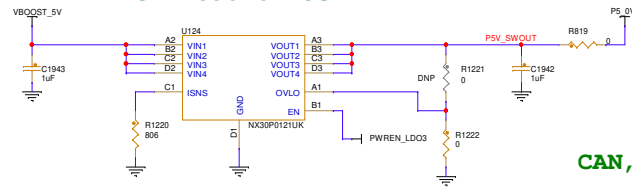
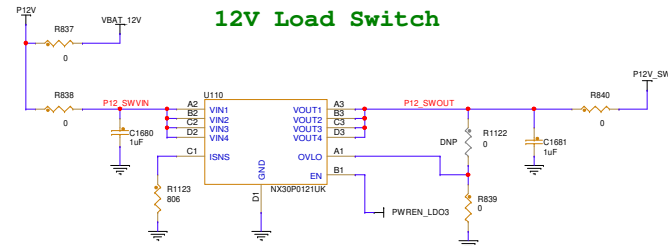
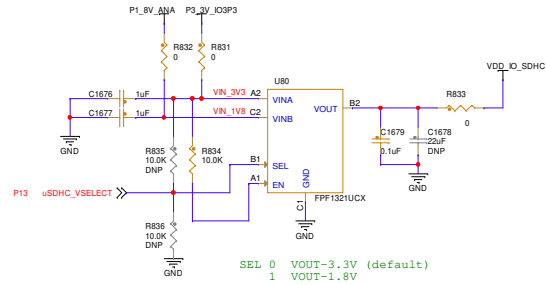


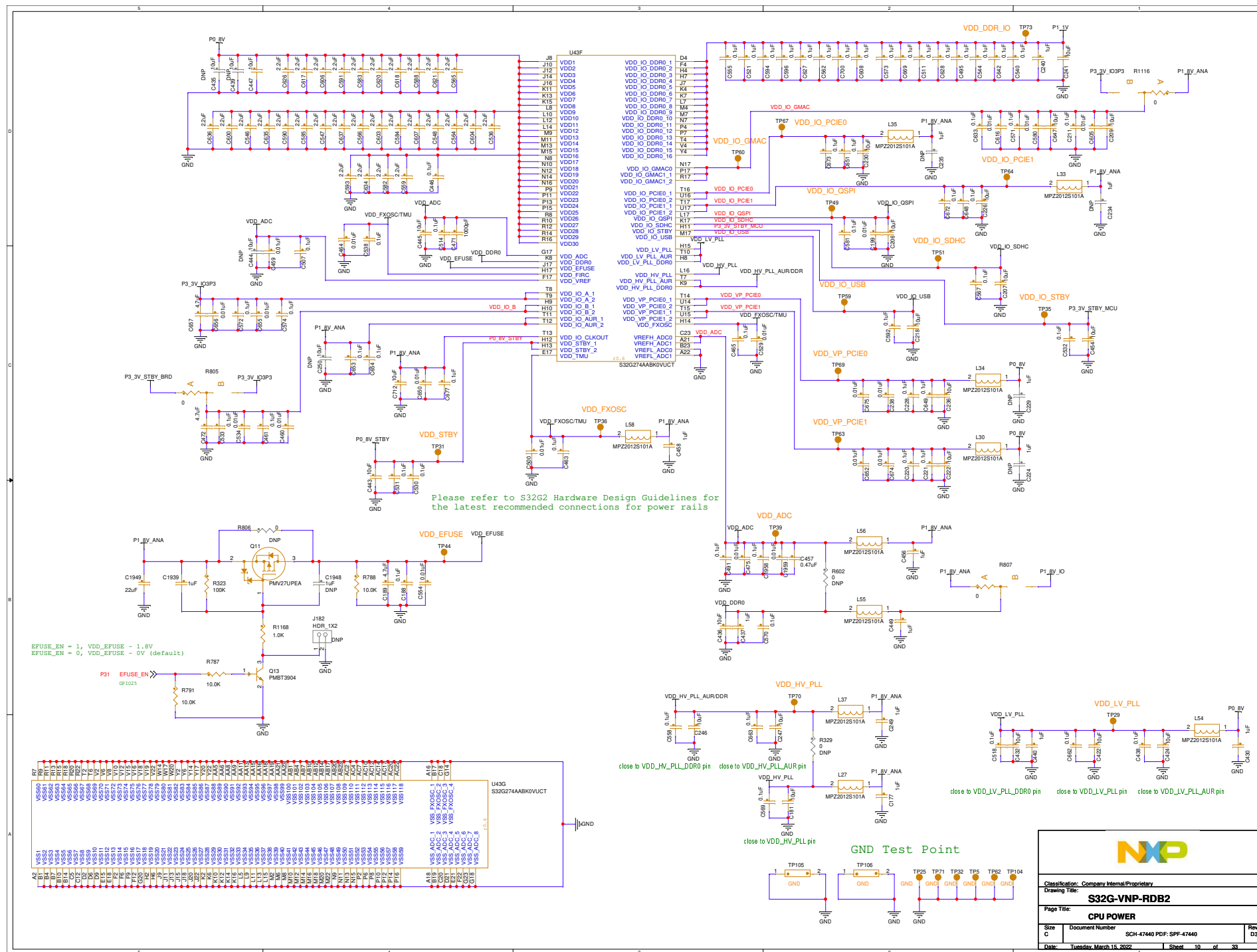
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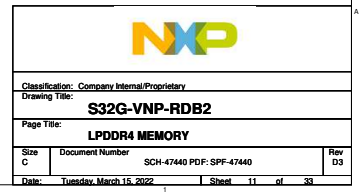
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CPU POWER

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MCU RESET CIRCUIT

The MCU Reset Circuit includes a POR (Power-On Reset) section with a SW1 switch and a PWR/RST section with a PWR/RST switch. The circuit also includes a RESET section with a SW2 switch. The reset signal is generated by a 74VHC1G17G0W NAND gate (U1) and a 74VHC1G17G0W NAND gate (U2). The reset signal is connected to the MCU's RESET pin (P6.12,20).

20-Pin JTAG

The 20-Pin JTAG interface is connected to the MCU's JTAG pins (P6.12,20). The JTAG pins are connected to a 20-pin connector (J48) and a 20-pin header (H01_2X10).

AURORA

The AURORA module is connected to the MCU's AURORA pins (P6.12,20). The AURORA pins are connected to a 20-pin connector (J48) and a 20-pin header (H01_2X10).

RTC

The RTC (Real-Time Clock) module is connected to the MCU's RTC pins (P6.12,20). The RTC pins are connected to a 20-pin connector (J48) and a 20-pin header (H01_2X10).

TEMP SENSOR

The Temperature Sensor module is connected to the MCU's TEMP pins (P6.12,20). The TEMP pins are connected to a 20-pin connector (J48) and a 20-pin header (H01_2X10).

Pin List for S32G274AABK0VUCT

Pin	Signal	Pin	Signal
AC11	AUR_CLKP	AC12	AUR_CLKN
AC13	AUR_TX0_P	AC14	AUR_TX0_N
AC15	AUR_TX1_P	AC16	AUR_TX1_N
AC17	AUR_TX2_P	AC18	AUR_TX2_N
AC19	AUR_TX3_P	AC20	AUR_TX3_N
AC21	AUR_TX4_P	AC22	AUR_TX4_N
AC23	AUR_TX5_P	AC24	AUR_TX5_N
AC25	AUR_TX6_P	AC26	AUR_TX6_N
AC27	AUR_TX7_P	AC28	AUR_TX7_N
AC29	AUR_TX8_P	AC30	AUR_TX8_N
AC31	AUR_TX9_P	AC32	AUR_TX9_N
AC33	AUR_TX10_P	AC34	AUR_TX10_N
AC35	AUR_TX11_P	AC36	AUR_TX11_N
AC37	AUR_TX12_P	AC38	AUR_TX12_N
AC39	AUR_TX13_P	AC40	AUR_TX13_N
AC41	AUR_TX14_P	AC42	AUR_TX14_N
AC43	AUR_TX15_P	AC44	AUR_TX15_N
AC45	AUR_TX16_P	AC46	AUR_TX16_N
AC47	AUR_TX17_P	AC48	AUR_TX17_N
AC49	AUR_TX18_P	AC50	AUR_TX18_N
AC51	AUR_TX19_P	AC52	AUR_TX19_N
AC53	AUR_TX20_P	AC54	AUR_TX20_N
AC55	AUR_TX21_P	AC56	AUR_TX21_N
AC57	AUR_TX22_P	AC58	AUR_TX22_N
AC59	AUR_TX23_P	AC60	AUR_TX23_N
AC61	AUR_TX24_P	AC62	AUR_TX24_N
AC63	AUR_TX25_P	AC64	AUR_TX25_N
AC65	AUR_TX26_P	AC66	AUR_TX26_N
AC67	AUR_TX27_P	AC68	AUR_TX27_N
AC69	AUR_TX28_P	AC70	AUR_TX28_N
AC71	AUR_TX29_P	AC72	AUR_TX29_N
AC73	AUR_TX30_P	AC74	AUR_TX30_N
AC75	AUR_TX31_P	AC76	AUR_TX31_N
AC77	AUR_TX32_P	AC78	AUR_TX32_N
AC79	AUR_TX33_P	AC80	AUR_TX33_N
AC81	AUR_TX34_P	AC82	AUR_TX34_N
AC83	AUR_TX35_P	AC84	AUR_TX35_N
AC85	AUR_TX36_P	AC86	AUR_TX36_N
AC87	AUR_TX37_P	AC88	AUR_TX37_N
AC89	AUR_TX38_P	AC90	AUR_TX38_N
AC91	AUR_TX39_P	AC92	AUR_TX39_N
AC93	AUR_TX40_P	AC94	AUR_TX40_N
AC95	AUR_TX41_P	AC96	AUR_TX41_N
AC97	AUR_TX42_P	AC98	AUR_TX42_N
AC99	AUR_TX43_P	AC100	AUR_TX43_N

I2C Address: 1010001R/W 0x51

I2C Address: 1001000R/W 0x48

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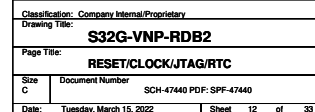
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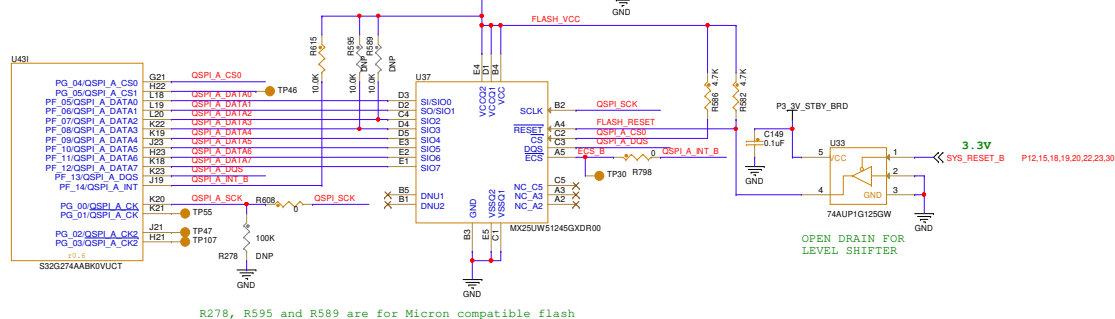
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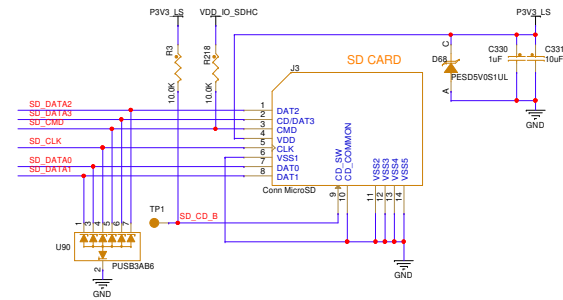
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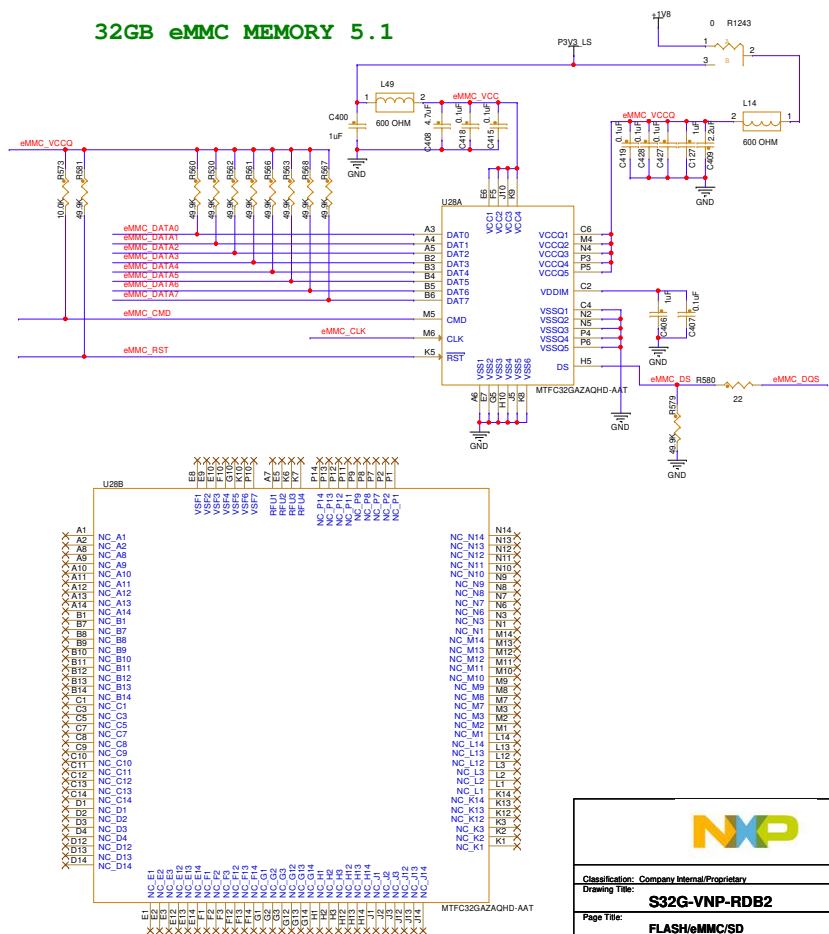
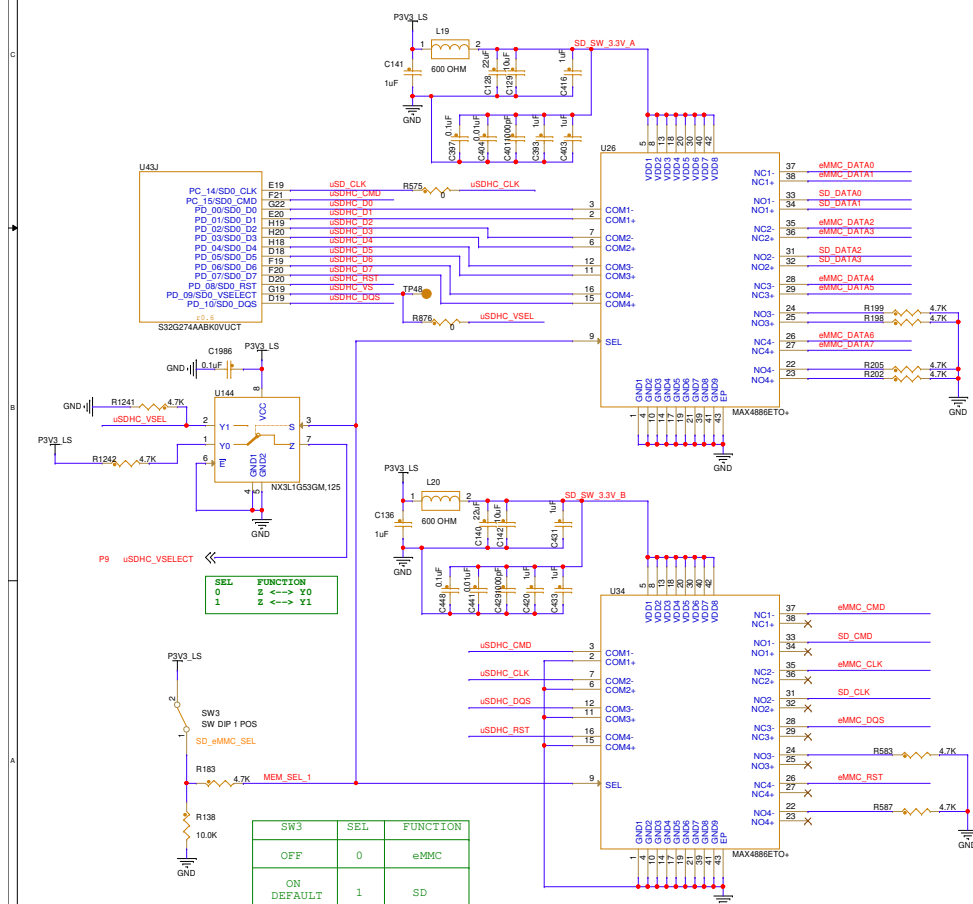
MICRO SD CARD SOCKET



R278, R595 and R589 are for Micron compatible flash



32GB eMMC MEMORY 5.1



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Drawing Title:

S32G-VNP-RDB2

Page Title: **FLASH/eMMC/SD**

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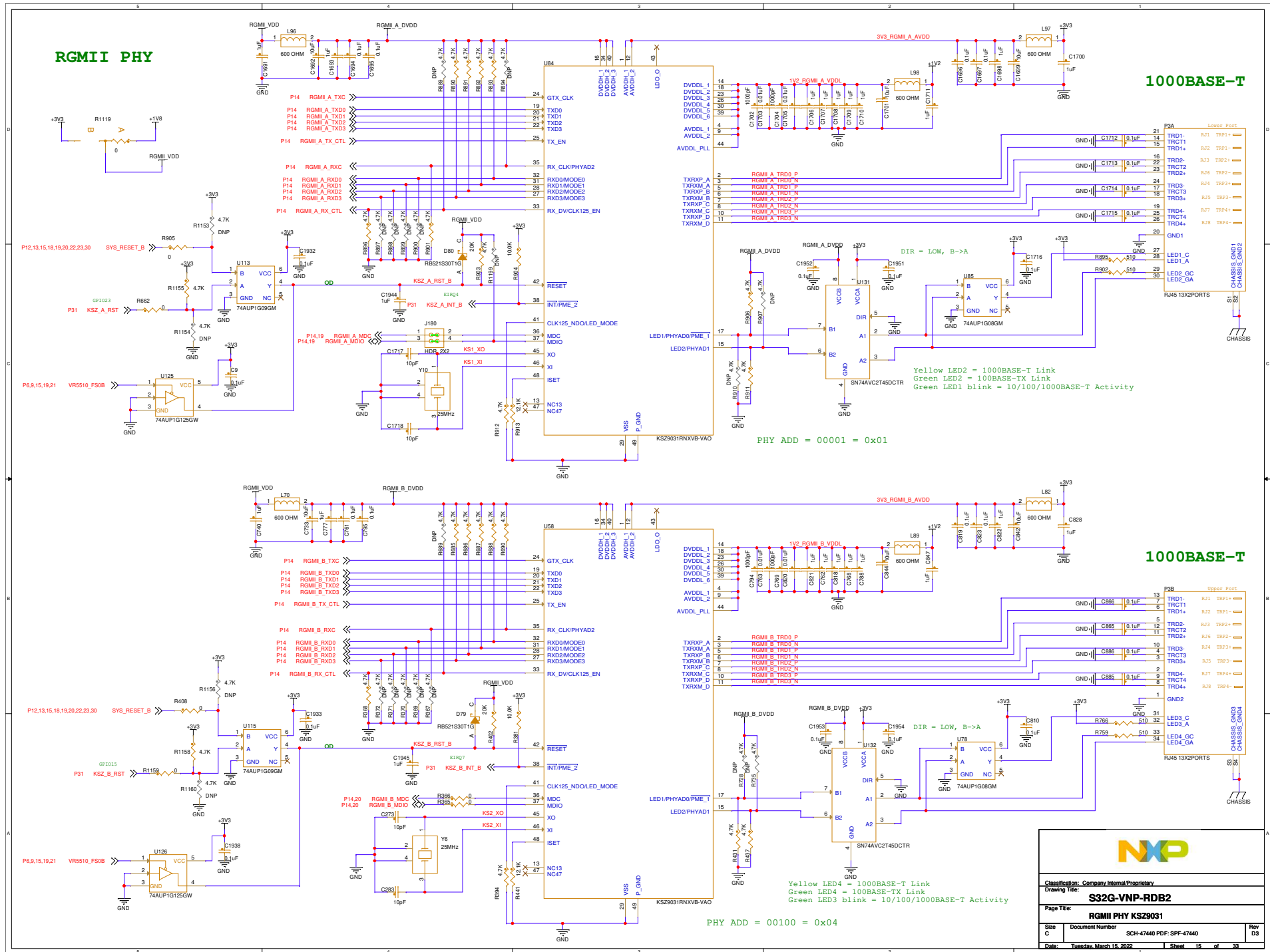
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RGMII PHY

1000BASE-T



The diagram shows a detailed PCB layout for a PCIe-to-USB4 adapter. Key components and their connections are as follows:

- U43C (S32G274AABK8VUCT):** PCIe controller. Pins include PCIE0_CLK_P, PCIE0_CLK_N, PCIE0_RX0_P, PCIE0_RX0_N, PCIE0_RX1_P, PCIE0_RX1_N, PCIE0_TX0_P, PCIE0_TX0_N, PCIE0_TX1_P, PCIE0_TX1_N, PCIE0_REXT, and PCIE0_RXN. It is connected to a SW17 switch and a SW DIP 1 POS.
- U402 (AA22):** PCIe-to-USB4 bridge. Pins include PCIE1_RX0_P, PCIE1_RX0_N, PCIE1_RX1_P, PCIE1_RX1_N, PCIE1_TX0_P, PCIE1_TX0_N, PCIE1_TX1_P, PCIE1_TX1_N, and PCIE1_RXN. It is connected to U43C and U102.
- U102 (U102):** USB4 controller. Pins include VDD1, VDD2, VDD3, B0_P, B0_N, B1_P, B1_N, C0_P, C0_N, C1_P, C1_N, SEL, and XSD. It is connected to U402 and U104.
- U104 (U104):** USB4 controller. Pins include VDD1, VDD2, VDD3, B0_P, B0_N, B1_P, B1_N, C0_P, C0_N, C1_P, C1_N, SEL, and XSD. It is connected to U102 and U104.
- U112 (74VC1G04W-Q100):** Inverter. Pins include VCC, GND, and Y. It is connected to U102 and U104.
- U104 (CBLT02043A):** USB4 controller. Pins include VDD1, VDD2, VDD3, B0_P, B0_N, B1_P, B1_N, C0_P, C0_N, C1_P, C1_N, SEL, and XSD. It is connected to U102 and U104.

The layout includes various signal traces, power planes, and component footprints. Labels include component names (U43C, U402, U102, U104), pin numbers, and signal names (PCIE0_CLK_P, PCIE0_CLK_N, etc.).

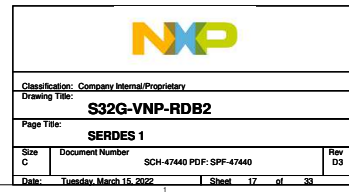
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	SW17	Mode	PHY Lan		Connection	SerDes_0 reference clock (External)
SerDes_0	OFF	PCIe only mode	LaNo, Lan1	PCIe0_X2 mode	M.2 E-key slot	100M
	ON (Default)	PCIe only mode	LaNo, Lan1	PCIe0_X2 mode	M.2 M-key slot	100M
	SW8	Mode	PHY Lan		Connection	SerDes_1 reference clock (External)
SerDes_1	OFF	PCIe/SGMII mode	LaNo	PCIe X1 mode	PCIe X1 socket	100M
			Lan1	SGMII 1.25 Gbps (PFE_MAC0 or PFE_MAC1)	SJA1110	
	ON (Default)	SGMII mode1	LaNo	SGMII 1.25 Gbps (PFE_MAC0)	SJA1110	125M
			Lan1	SGMII 1.25 Gbps (PFE_MAC1)	AQR113C	
		SGMII mode2	LaNo	SGMII 3.125 Gbps (PFE_MAC0)	SJA1110	
			Lan1	S32G2 : Not available	NA	
				S32G3 : SGMII 3.125 Gbps (PFE_MAC1)	AQR113C	

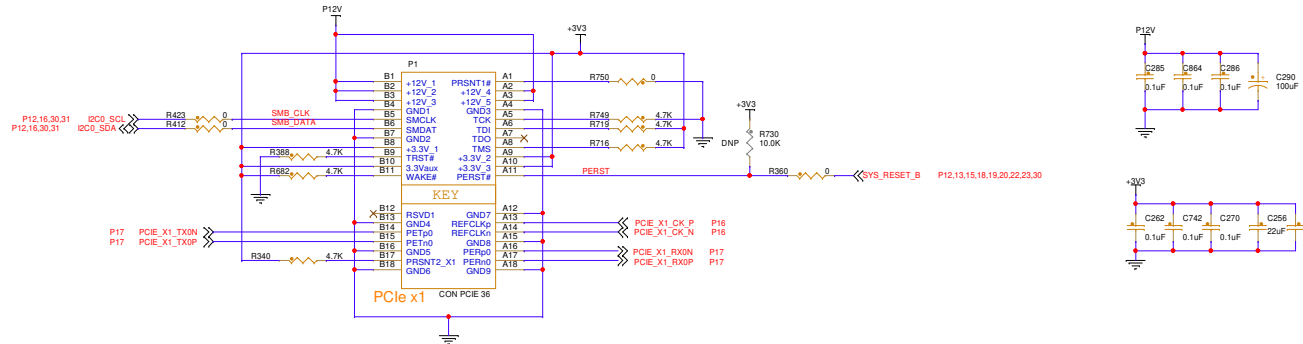


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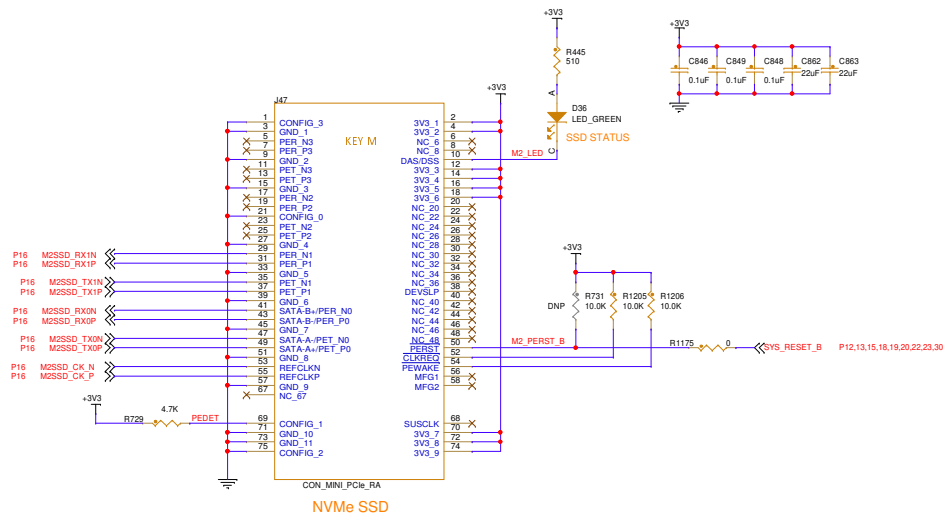
Refer to the table on Page 16 for the options



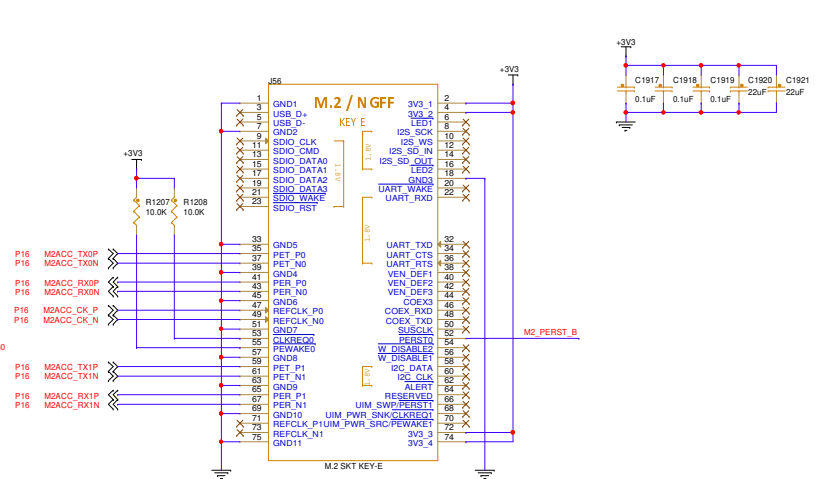
PCIe X1 Connector



M.2 Connector
PCIe x2 SSD 2242 (KEY M)



M.2 Connector
PCIe x2 2230 (KEY E)



M.2 Card Mounting Hole



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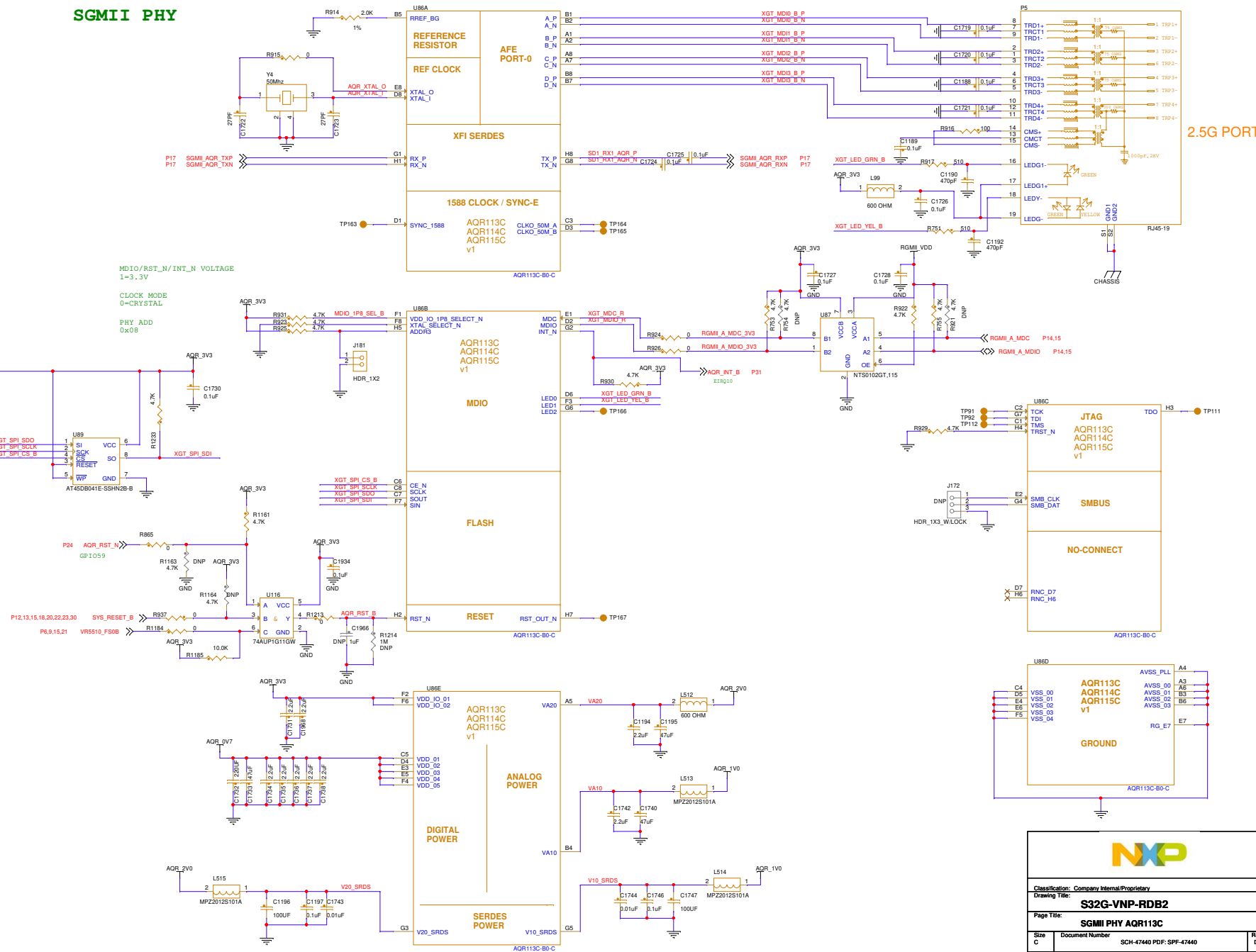
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Size C	Document Number SCH-47440 PDF: SPF-47440
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Rev
D3

SGMII PHY



2.5G PORT



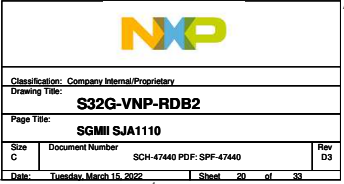
Classification: Company Internal/Proprietary

Drawing Title: **S32G-VNP-RDB2**

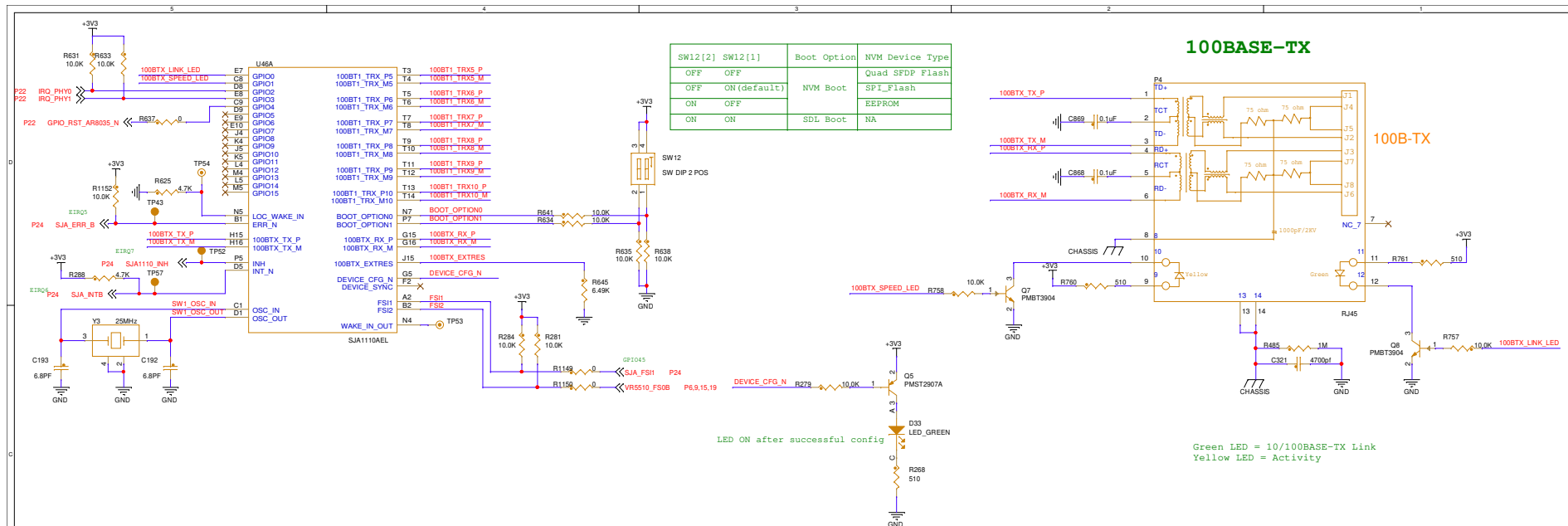
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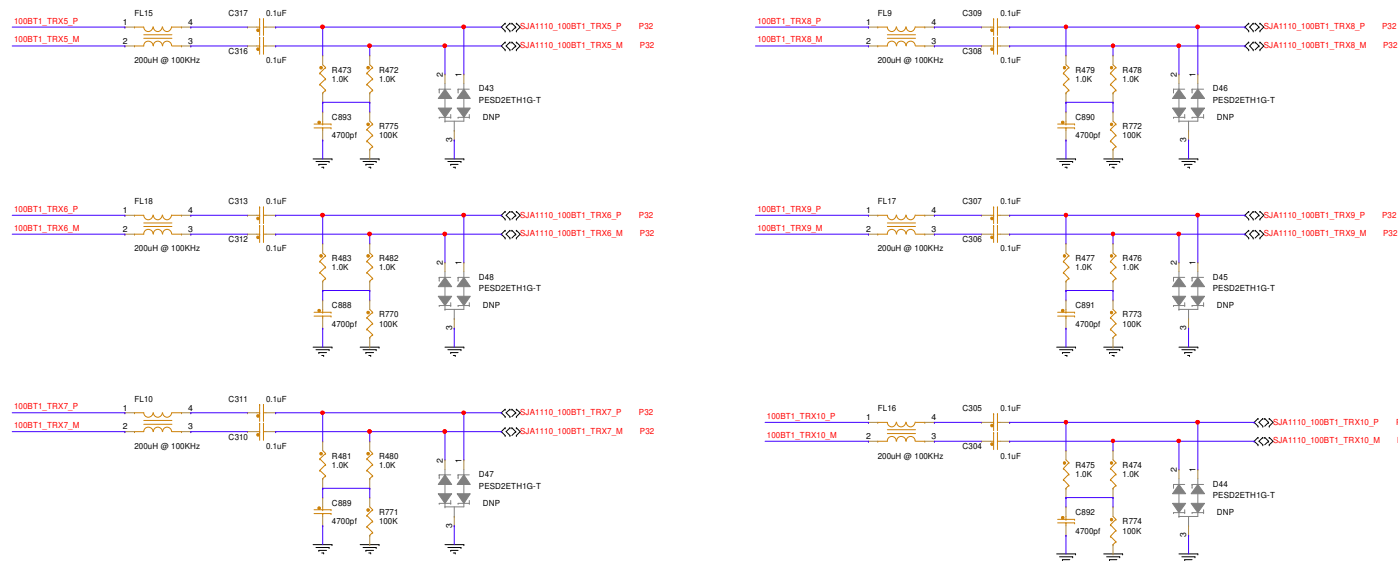
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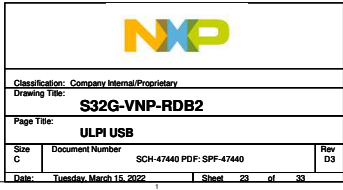


100BASE-TX

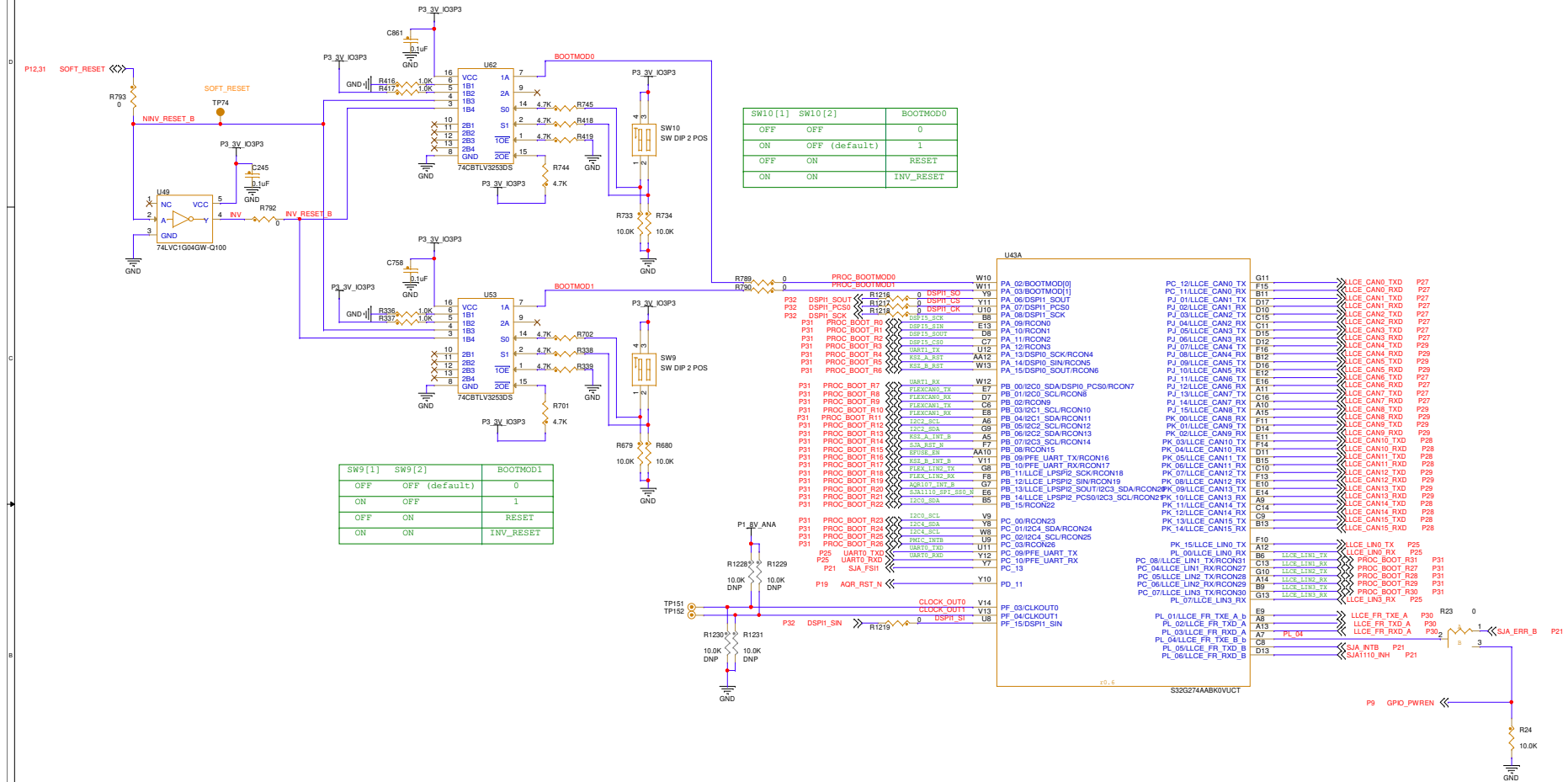


100BASE-T1

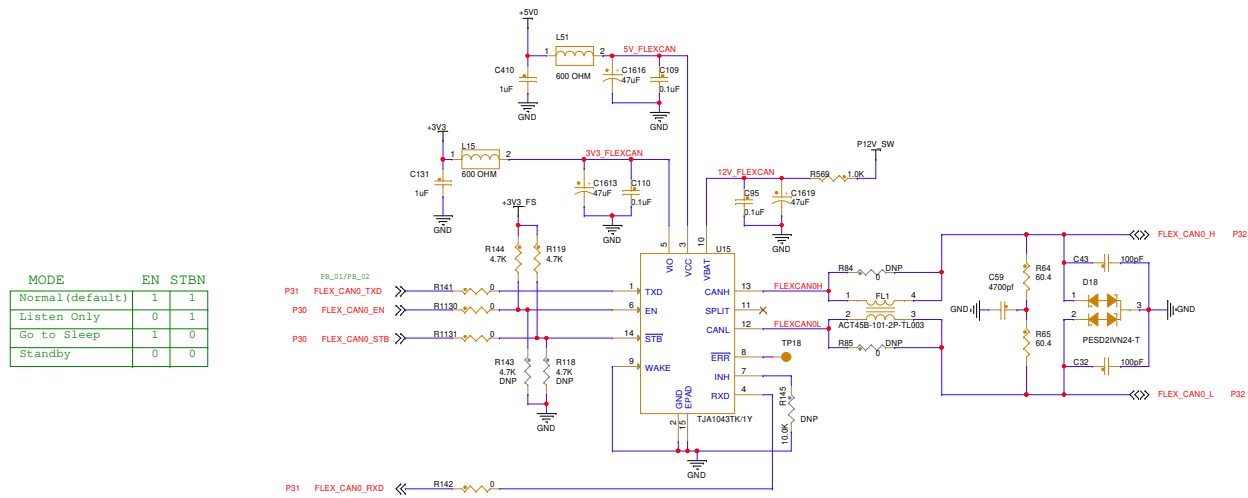




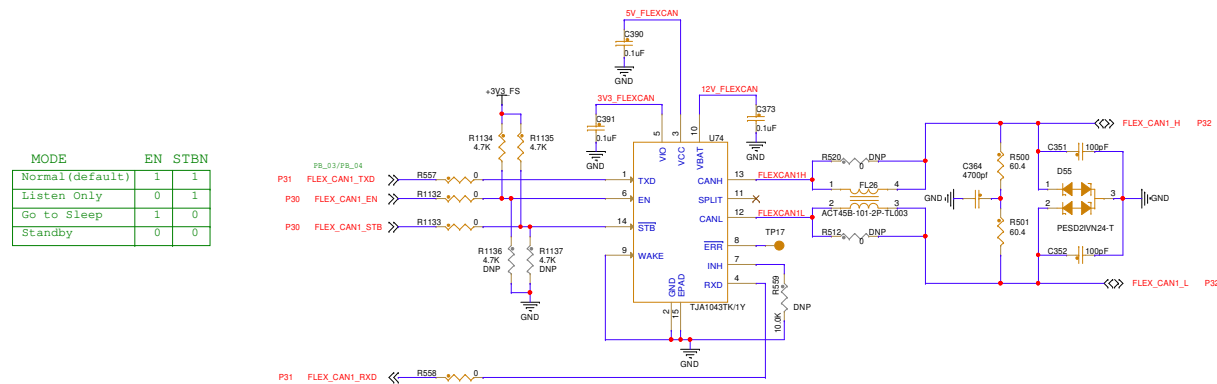
Boot Mode Select



CAN OTHER2 DOMAIN



CAN ODB DOMAIN



Classification: Company Internal/Proprietary

Drawing Title: S32G-VNP-RDB2

Page Title: FLEX CAN

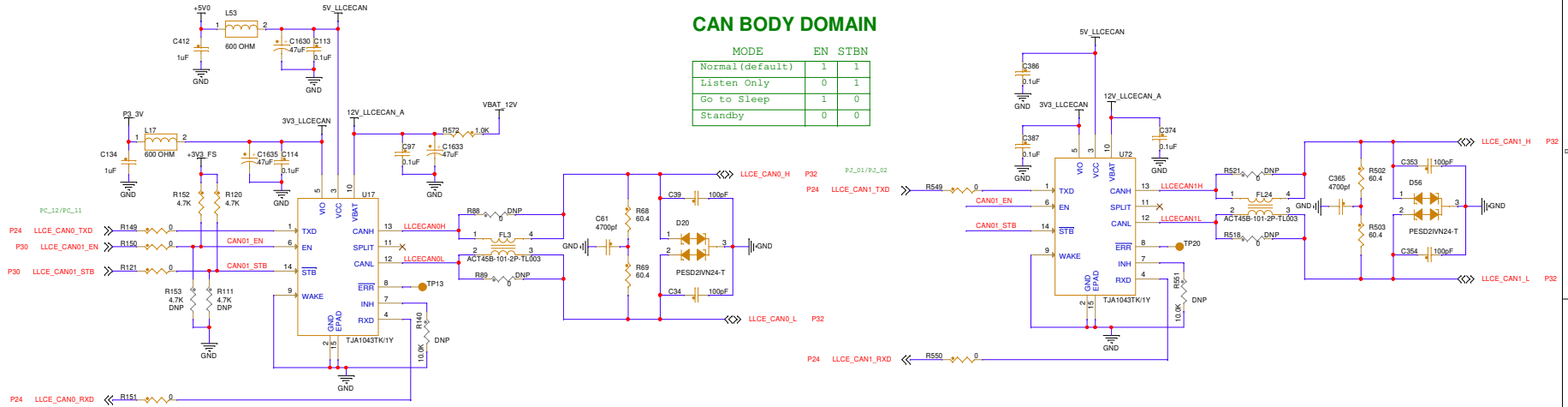
Size C Document Number SCH-47440 PDF: SPF-47440

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Rev 03

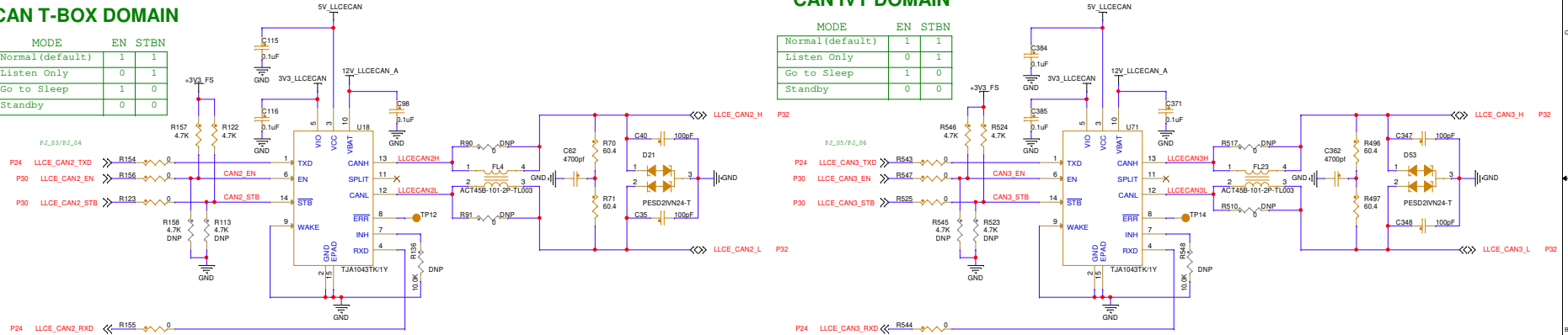
CAN BODY DOMAIN

MODE	EN	STBN
Normal (default)	1	1
Listen Only	0	1
Go to Sleep	1	0
Standby	0	0



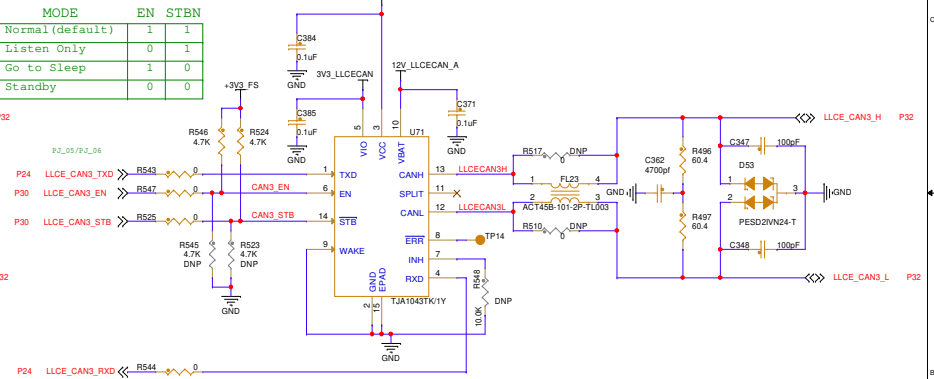
CAN T-BUS DOMAIN

MODE	EN	STBN
Normal (default)	1	1
Listen Only	0	1
Go to Sleep	1	0
Standby	0	0



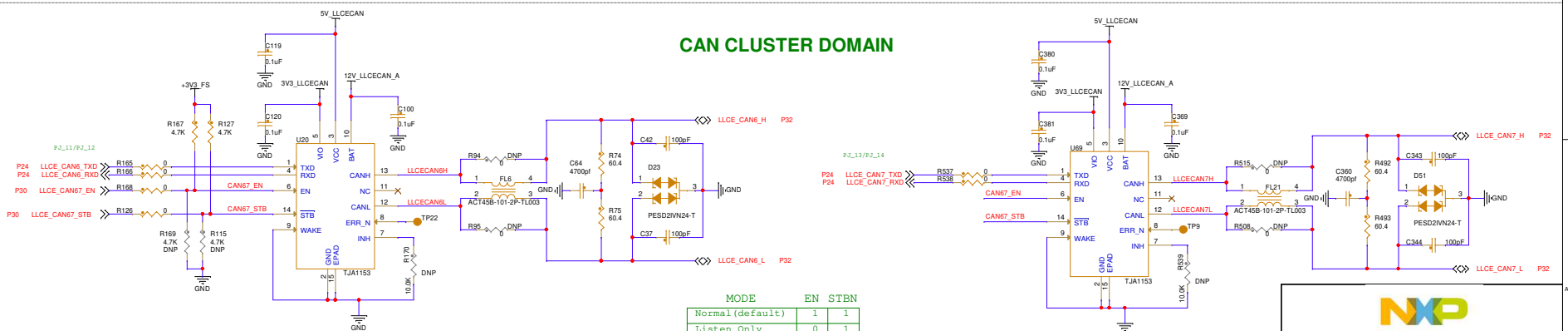
CAN IVT DOMAIN

MODE	EN	STBN
Normal (default)	1	1
Listen Only	0	1
Go to Sleep	1	0
Standby	0	0

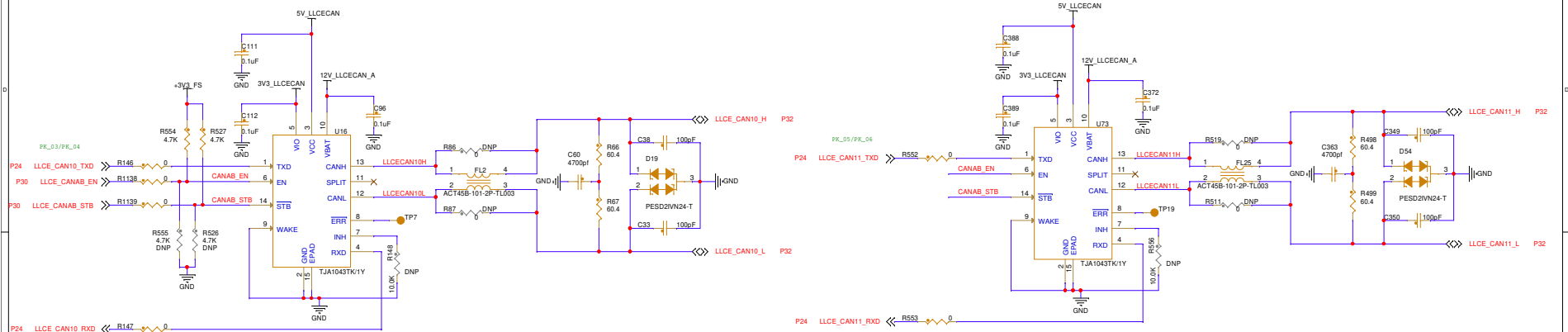


CAN CLUSTER DOMAIN

MODE	EN	STBN
Normal (default)	1	1
Listen Only	0	1
Go to Sleep	1	0
Standby	0	0

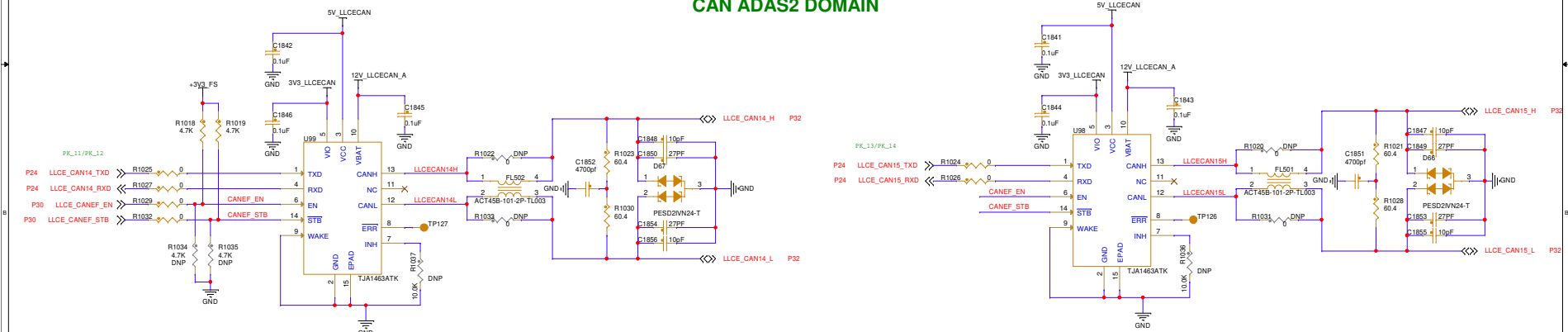


CAN OTHER DOMAIN



MODE	EN	STBN
Normal(default)	1	1
Listen Only	0	1
Go to Sleep	1	0
Standby	0	0

CAN ADAS2 DOMAIN



MODE	EN	STBN
Normal(default)	1	1
Listen Only	0	1
Go to Sleep	1	0
Standby	0	0



Classification: Company Internal/Proprietary

Drawing Title: **S32G-VNP-RDB2**

Page Title: **LLCE CAN_2**

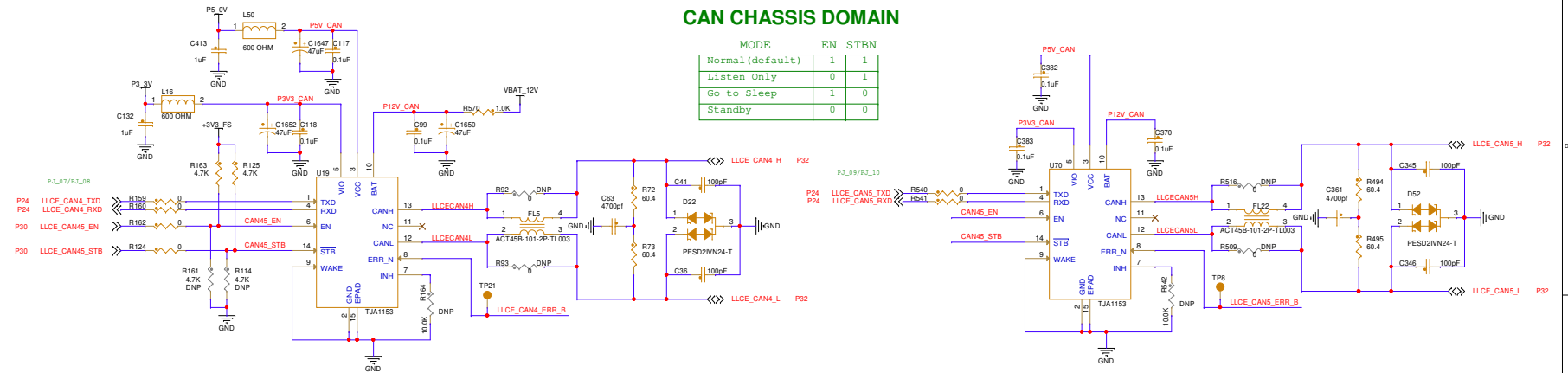
Size C Document Number SCH-47440 PDF: SPF-47440

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Rev 03

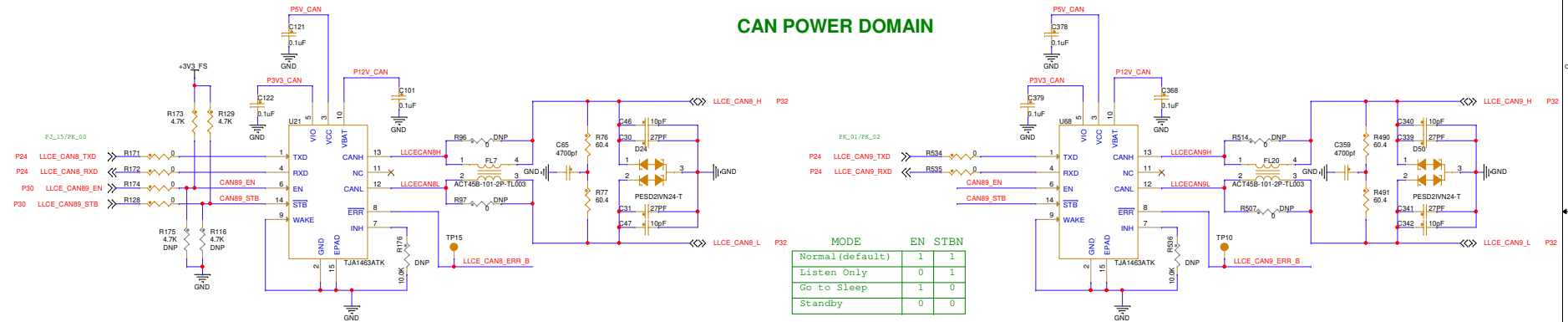
CAN CHASSIS DOMAIN

MODE	EN	STBN
Normal (default)	1	1
Listen Only	0	1
Go to Sleep	1	0
Standby	0	0



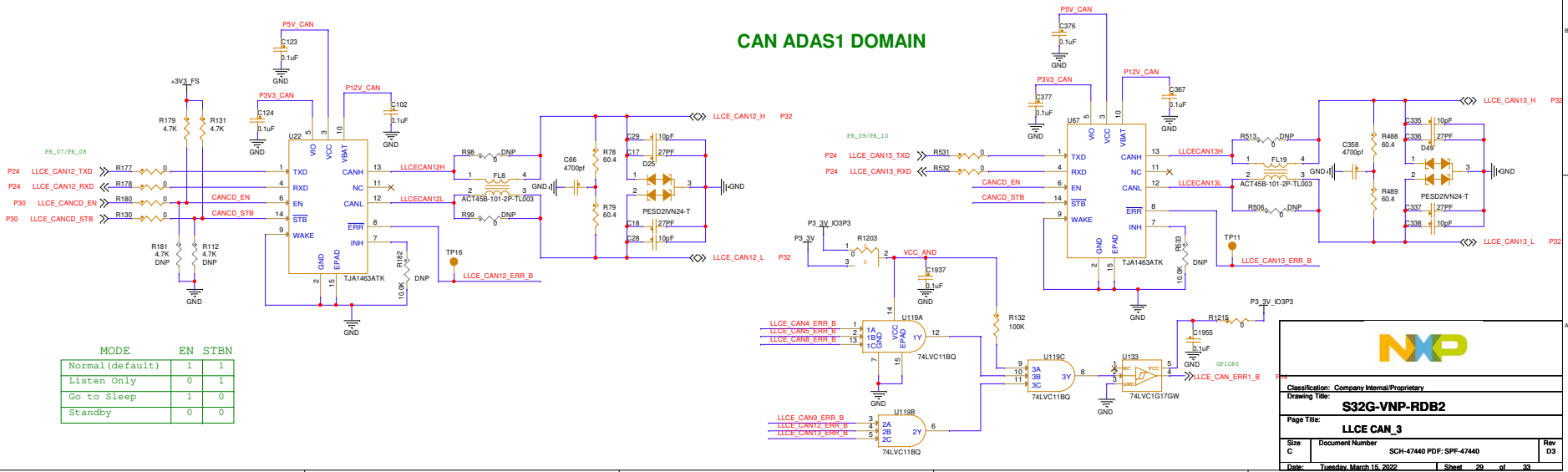
CAN POWER DOMAIN

MODE	EN	STBN
Normal (default)	1	1
Listen Only	0	1
Go to Sleep	1	0
Standby	0	0



CAN ADAS DOMAIN

MODE	EN	STBN
Normal (default)	1	1
Listen Only	0	1
Go to Sleep	1	0
Standby	0	0



Classification: Company Internal/Proprietary

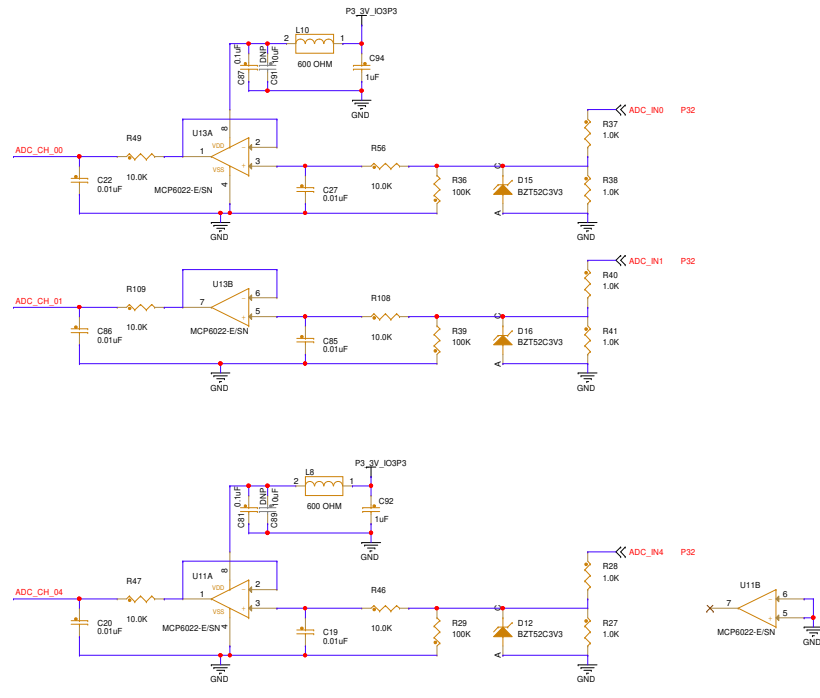
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Page Title: LLCE_CAN_3

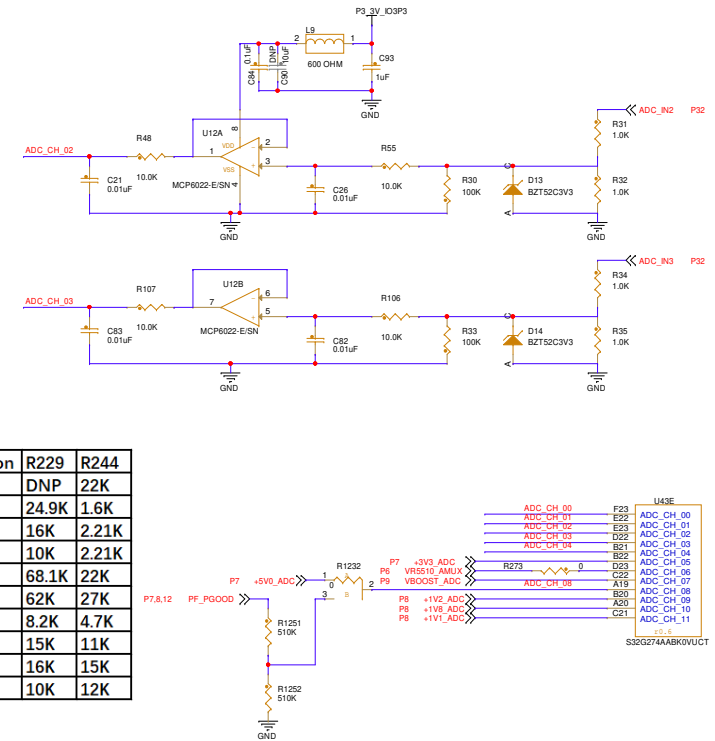
Size C Document Number SCH-47440 PDF: SPF-47440

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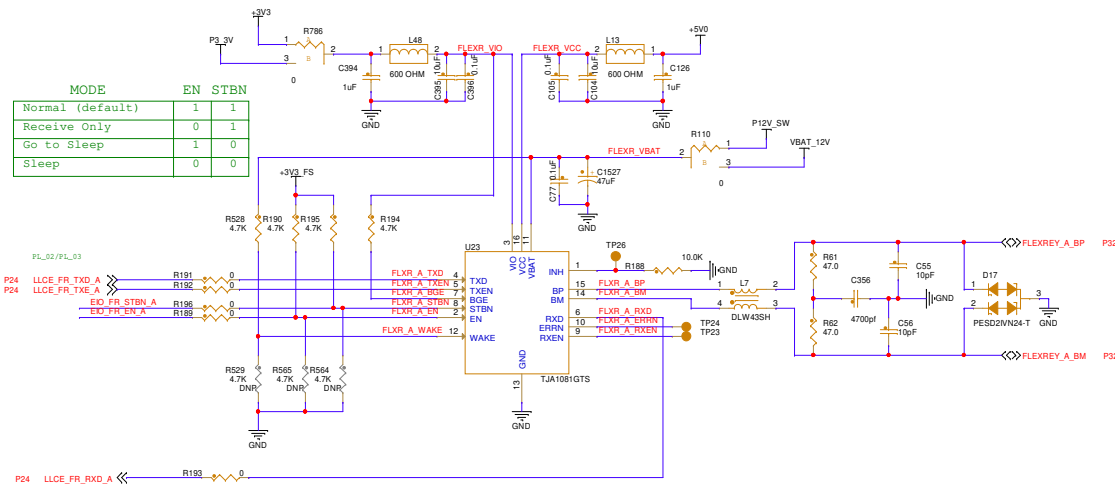
ADC



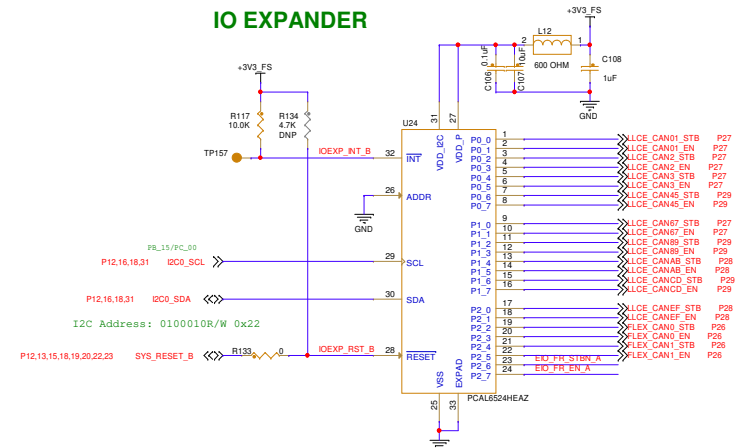
ADC CH 05	Board Version	R229	R244
0V		DNP	22K
0.2V		24.9K	1.6K
0.4V		16K	2.21K
0.6V		10K	2.21K
0.8V	Rev. C	68.1K	22K
1V	Rev. D	62K	27K
1.2V		8.2K	4.7K
1.4V		15K	11K
1.6V		16K	15K
1.8V		10K	12K



FLEXRAY



IO EXPANDER



Classification: Company Internal/Proprietary

Classification:
Drawing Title:

Page Title: **FLEXRAY/ADC/EXPAND_IO**

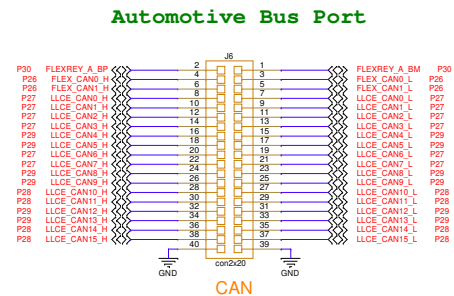
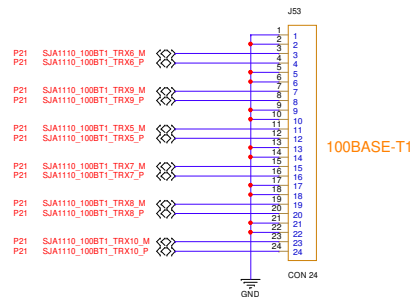
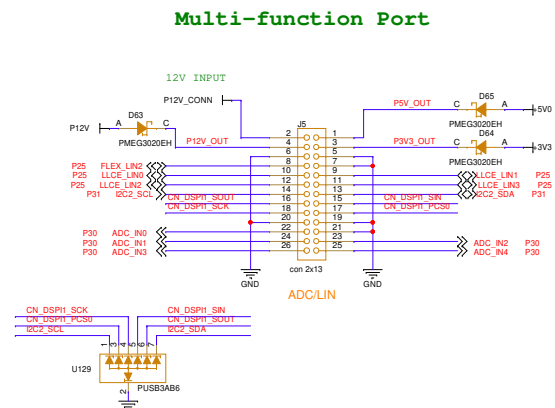
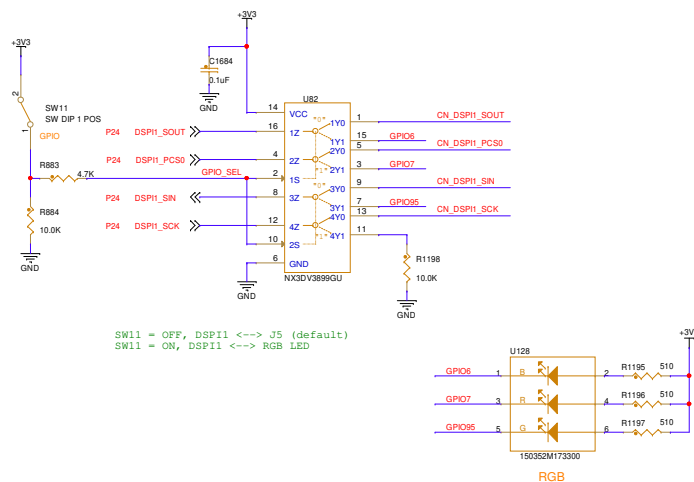
Size C	Document Number SCH-47440 PDF: SPF-47440
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[illegible]



Default Jumper setting:

REF DES	JUMPER(DEFAULT)	PAGE NAME
J184	1-2	06 POWER VR5510
R866,R868,R1193,R1200	A	06 POWER VR5510
R939,R940,R1192	A	07 PF5300 & FS5600
R812,R813	A	09 POWER JUMPER
R805,R807,R1116	A	10 CPU POWER
R1210,R1243	A	13 FLASH/eMMC/SD
J180	1-2, 3-4	15 RGMII PHY KSZ9031
R1119	A	15 RGMII PHY KSZ9031
R357,R358,R361,R362	A	22 SGMII SJA1110 1000BASE-T
R23	A	24 S32G PORT
R1203	A	29 LLCE CAN 3
R1110,R786,R1232	A	30 FLEXRAY/ADC/EXPAND IO

Default Switch setting:

REF DES	SWITCH(DEFAULT)	PAGE NAME
SW15	OFF	06 POWER VR5510
SW3	ON	13 FLASH/eMMC/SD
SW8,SW17	ON	16 PCIECLK/SERDES 0
SW12	1-ON, 2-OFF	21 SGMII SJA1110 100BASE-T1/TX
SW9	1-OFF, 2-OFF	24 S32G PORT
SW10	1-ON, 2-OFF	24 S32G PORT
SW5,SW6,SW7	1-OFF, 2-OFF, 3-OFF, 4-OFF, 5-OFF, 6-OFF, 7-OFF, 8-OFF	31 RCON BOOT
SW4	1-OFF, 2-OFF, 3-OFF, 4-OFF, 5-OFF, 6-OFF, 7-ON, 8-OFF	31 RCON BOOT
SW11	OFF	32 CONNECTORS



Classification: Company Internal/Proprietary

Drawing Title: **S32G-VNP-RDB2**

Page Title: **DEFAULT JUMPER SETTING**

Size C Document Number SCH-47440 PDF: SPF-47440

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