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S32G-VNP-RDB

Reference Document:
Ballmap r0.6
IOMUX v1.100

THIS COLOR IS FOR SILK SCREEN TEXT

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Automotive Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

Designer: <Designer>	Drawing Title: S32G-VNP-RDB		
Drawn by: <DrawnBy>	Page Title: TITLE PAGE		
Approved: <Approver>	Size C	Document Number SCH-46384 PDF: SPF-46384	Rev B3
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Revision History

Revision	Date	Description
X1	SEP 2, 2019	Rev X1 Draft
A	SEP 27, 2019	Revision A release
A1	Nov 14, 2019	1. DNP R638, populate R641. 2. Change default jumper of J22 & J26 to 1-3, 2-4. 3. DNP R144, R119, R554, R527, R152, R120, R157, R122, R546, R524, R163, R125, R167, R127, R173, R129, R179, R131, R190, R195. 4. Populate J50.
B	Jan 2, 2020	1. Change all Jumpers to 0 ohm resistors 2. Change F1 from 12A to 7A 3. Add overvoltage protect circuit on P12V input 4. DNP R25, D9, R313 to reduce 12V power consumption in Standby Mode 5. Change D1 LED, Fan J50, U9 (LIN), R569 (CAN U15, U16, U73, U74) power supply from P12V to P12V_SW to reduce 12V power consumption in Standby Mode. 6. Change VR5510 VDDIO from VPRE_3V3 to LDO3_3V3 to reduce VR5510 VPRE_3V3 power consumption in Standby Mode. 7. Add 0 ohm resistors on U32, U27, U66, U64, U36, U6, U4, U1, U5, U33, U35, U30 power input for current measurement. 8. Change R576, R251 from 100K to 1M to reduce VR5510 P3_3V power consumption in Standby Mode. 9. Change P1_8V_IO_QSPI, U63 power supply from P1_8V_IO to P1_8V_ANA to reduce VR5510 LDO2_1V8 power consumption in DDR self-refresh mode. 10. DNP R230, R247 as VR5510 VBOOST is not used on the board. 11. Change 3.3V Load Switch U64 from NCV451 to NX5P2924BUK, PCIe Clock generator U59 from NBA3N5573MNTXG to SI6332DD11441-AM1 as the sourcing issue. 12. Add SDHC power selection load switch U80 and controlled by S32G uSDHC_VSELECT pin. 13. Add 12V Load Switch U81 to reduce 12V power conumption in Standby Mode. 14. Change VDD_IO_B from P3_3V_IO3P3 to P3_3V_STBY_BRD as the high leakage current on VR5510 LDO3_3V3 in Standby Mode. 15. Change VDD_DDR0 from P1_8V_ANA to P1_8V_IO for DDR self-refresh mode. 16. Change U4, U6, U62, U53, U49, U35, U30, U25, U31, U38, U44 power supply from P3_3V_STBY_BRD to P3_3V_SW to reduce VR5510 VPRE_3V3 power consumption in Standby mode. 17. DNP U4 signal delay circuit for SOFT_RESET. 18. Change R578 pull up from P3_3V_STBY_BRD to P3_3V_IO3P3 to reduce VR5510 VPRE_3V3 power consumption in Standby mode. 19. Change SW3, SW8 from 2-position to 1-position 20. Change R643, R240, R234, R274 from P3_3V to P3_3V_SW to reduce VR5510 VPRE_3V3 power consumption in Standby mode. 21. Change R756, R252, R253, L15 (CAN U15, U16, U73, U74) from P3_3V to +3V3 to reduce VR5510 VPRE_3V3 power consumption in Standby mode. 22. Add pull down optional resistors for U60, U61 CONFIG3~1 pins. 23. Add buffer U79 on U8 RESET pin as the high leakage current in Standby mode. 24. Swap GPIO170 and GPIO24 connection on PCIe clock and bus switches or J5 Pin12. 25. DNP R266 and populate R269 to use RESET_B for U46 reset. 26. Change UART0 port selection Jumpers to switch U82. 27. Populate R114, R119, R554, R527, R190 and R564. 28. Add 0ohm power selection for U23 (FlexRay) VIO and VBAT, and connect to P3_3V_SW and P12V_SW to reduce the power consumption in Standby Mode. 29. Change R240, R234 from 4.7K to 1.5K. 30. DNP U35 signal delay circuit for PMIC_VDD_OK. 31. Add diode on J5 pin7, pin8 and pin28 to avoid reverse power input.
B1	Jan 17, 2020	Populate R152, R120, R157, R122, R546, R524, R163, R125, R167, R127, R173, R129, R179 and R131 to set all CAN PHYs in normal mode by default.
B2	Feb 10, 2020	U59 doesn't support frequency real time change by GPIO. DNP R323, R888 and populate SW8, R363 to change to frequency change by switch.
B3	Apr 17, 2020	1. Update U41 with complete part number PVR5510AMDA8ES 2. Change J53, J54 from 9-2305390-9 (210-81762) to 2305390-1 (210-82491), pin to pin compatible

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Page Title: REVISION HISTORY

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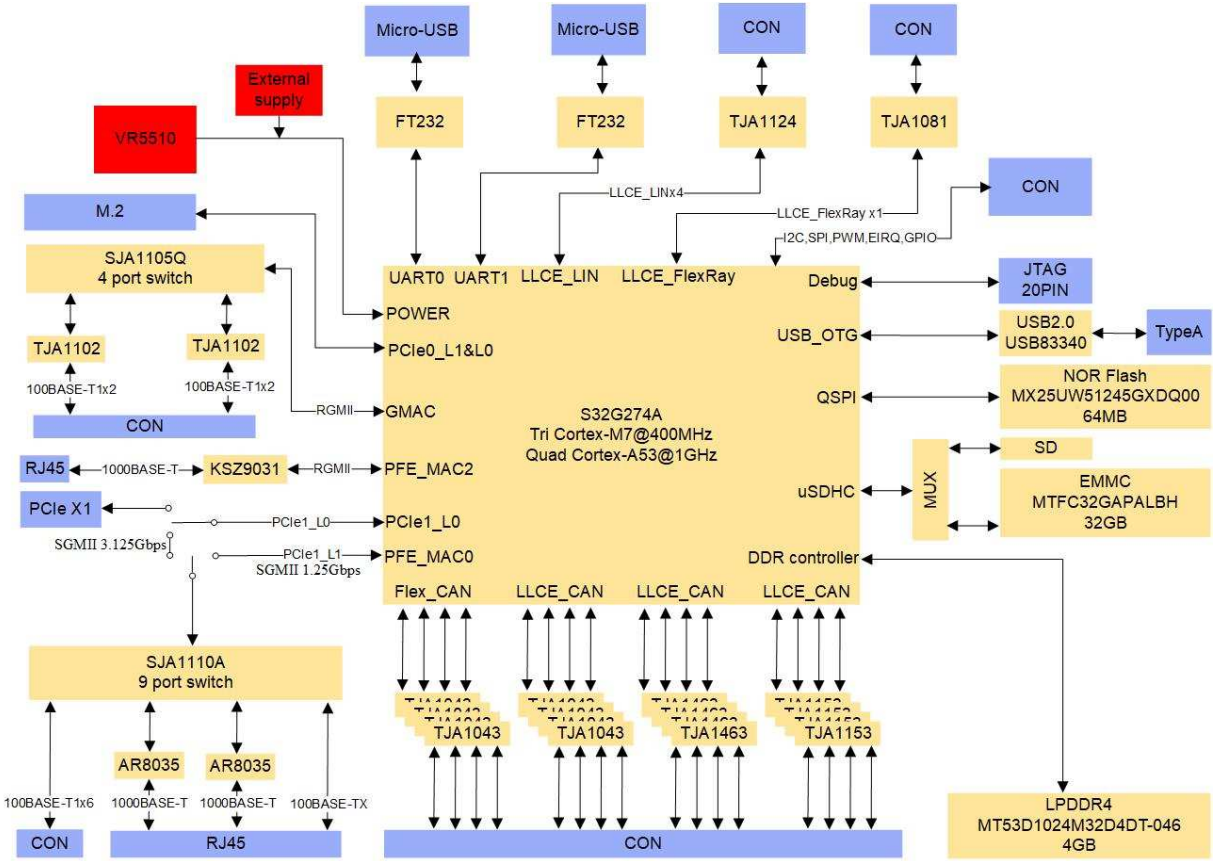

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Drawing Title: S32G-VNP-RDB

Page Title: BLOCK DIAGRAM

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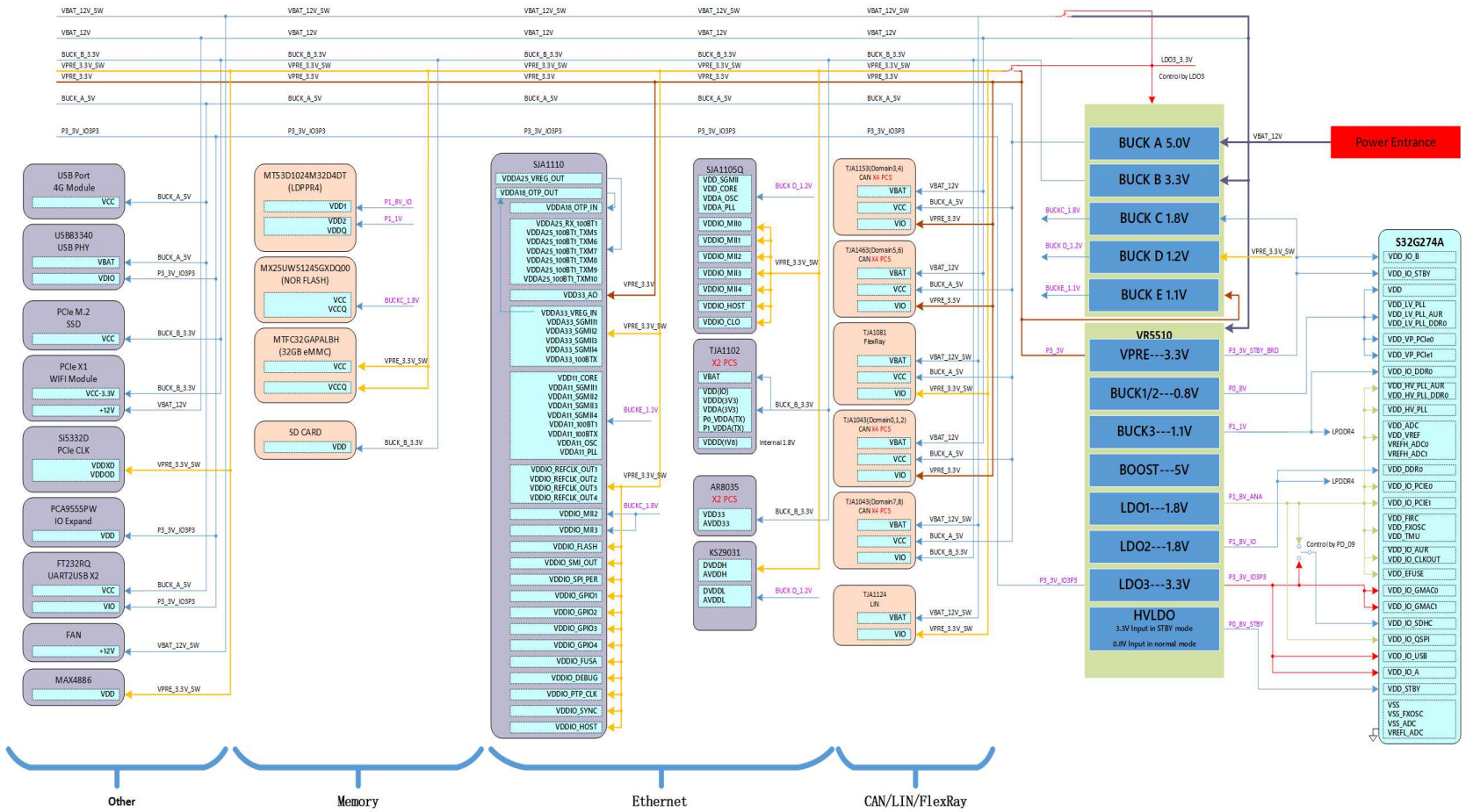

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Drawing Title: **S32G-VNP-RDB**

Page Title: **POWER TREE**

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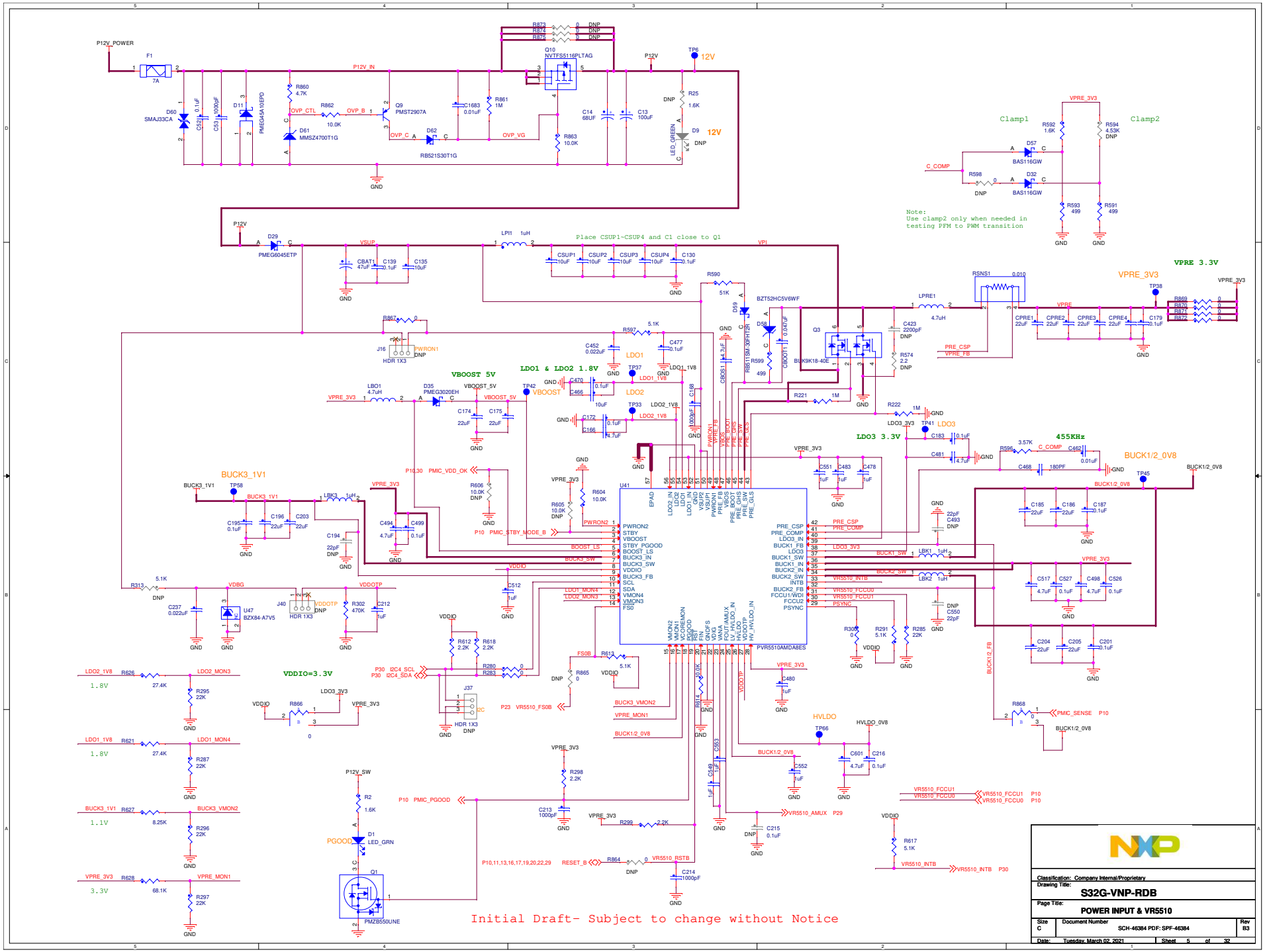
P12V_POWER
P12V_IN
P12V
12V
VSUP
VPI
VPRE_3V3
VPRE 3.3V
VBOOST 5V
LDO1 & LDO2 1.8V
LDO3 3.3V
455Khz
BUCK3_1V1
BUCK1/2_0V8
VDDIO=3.3V
HVLDO
Clamp1
Clamp2
Note:
Use clamp2 only when needed in testing PFM to PWM transition
Place CSUP1~CSUP4 and C1 close to Q1
PGOOD
LED_GRN
PMZB550UNE
PVR5510AMDA8ES
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POWER INPUT & VR5510
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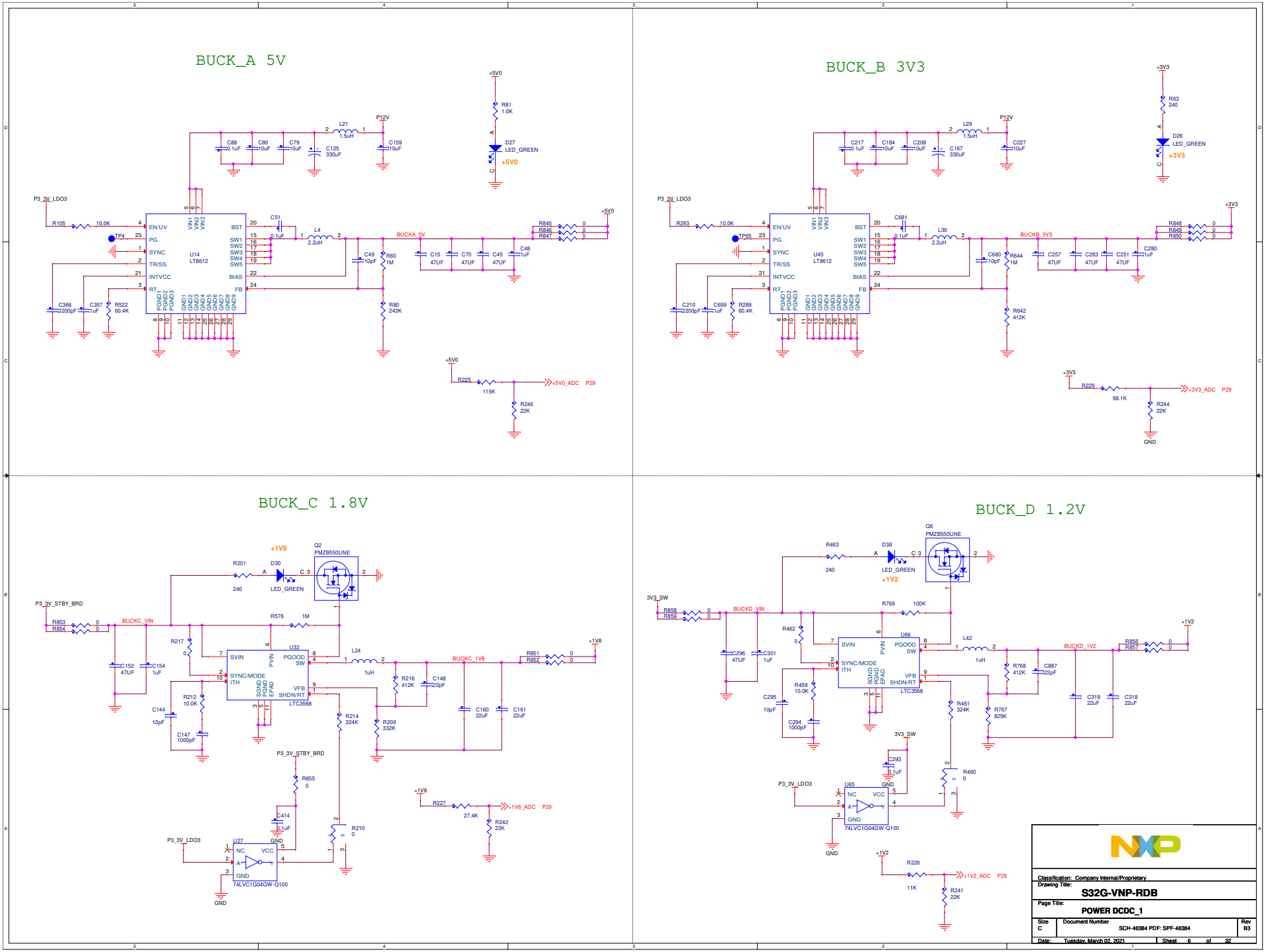
BUCK_A 5V
BUCK_B 3V3
BUCK_C 1.8V
BUCK_D 1.2V
LT8612
LTC3568
74LVC1G04GW-Q100
PMZB550UNE
LED_GREEN
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Page Title:
POWER DCDC_1
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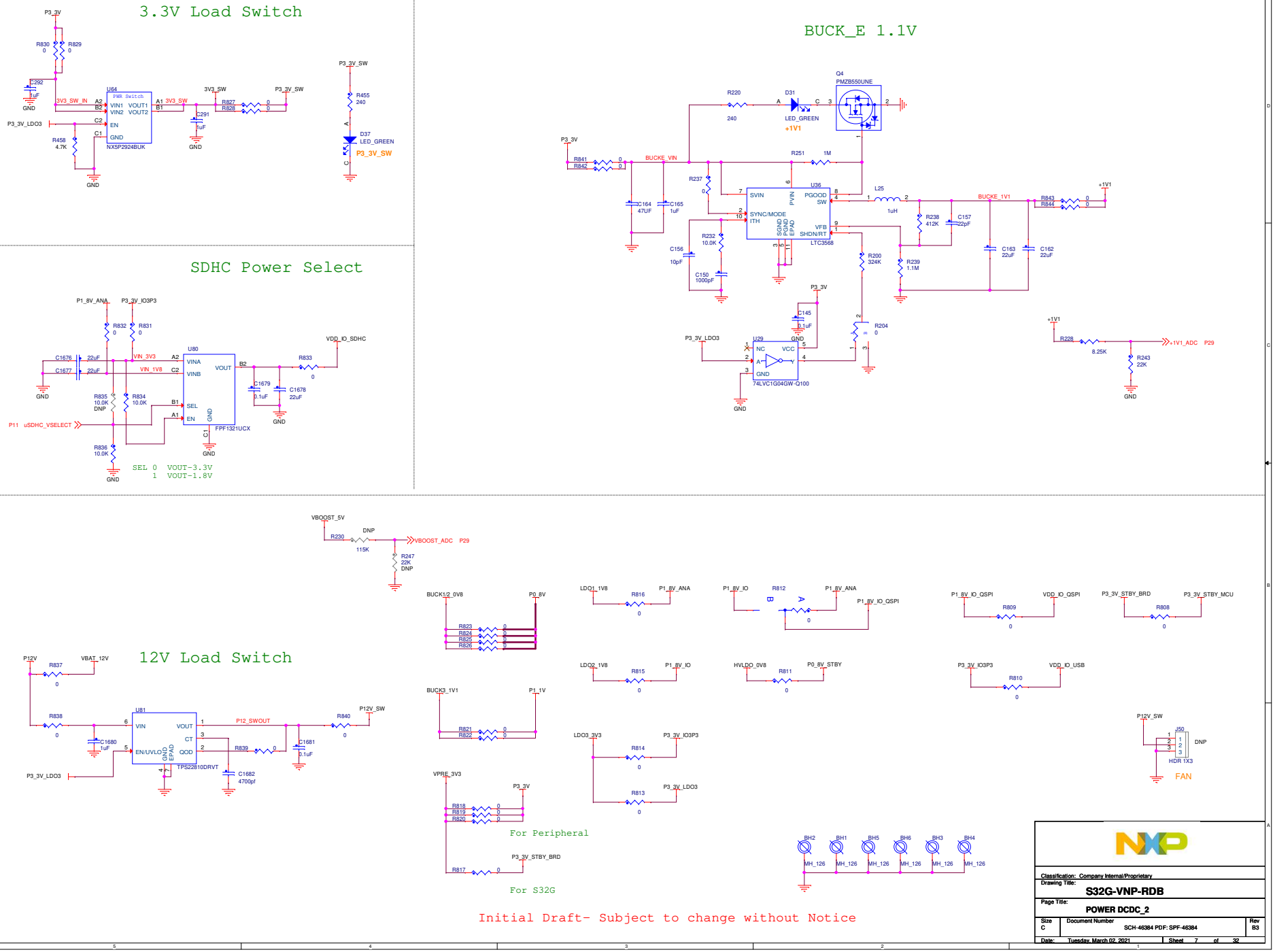
3.3V Load Switch
P3_3V
R830 0
R829 0
C292 1uF
GND
3V3_SW_IN
U64
PWR Switch
VIN1 VOUT1
VIN2 VOUT2
EN
GND
NX5P2924BUK
A1 3V3_SW
B1
C2
C1
P3_3V_LDO3
R458 4.7K
3V3_SW
R827 0
R828 0
P3_3V_SW
C291 1uF
P3_3V_SW
R455 240
D37
LED_GREEN
P3_3V_SW
SDHC Power Select
P1_8V_ANA
P3_3V_IO3P3
R832 0
R831 0
C1676 22uF
C1677 22uF
VIN_3V3
VIN_1V8
U80
VINA
VINB
VOUT
SEL
EN
GND
FPF1321UCX
VDD_IO_SDHC
R833 0
C1679 0.1uF
C1678 22uF
R835 10.0K DNP
R834 10.0K
P11 uSDHC_VSELECT
R836 10.0K
SEL 0 VOUT-3.3V
1 VOUT-1.8V
BUCK_E 1.1V
R220 240
D31
LED_GREEN
+1V1
Q4
PMZB550UNE
P3_3V
R841 0
R842 0
BUCKE_VIN
R251 1M
R237 0
U36
SVIN
PVIN
PGOOD
SW
SYNC/MODE
ITH
SGND
PGND
EPAD
VFB
SHDN/RT
LTC3568
L25
1uH
BUCKE_1V1
R843 0
R844 0
+1V1
C164 47UF
C165 1uF
R238 412K
C157 22pF
C163 22uF
C162 22uF
R232 10.0K
C156 10pF
C150 1000pF
R200 324K
R239 1.1M
P3_3V
C145 0.1uF
R204 0
P3_3V_LDO3
U29
NC
VCC
A
Y
GND
74LVC1G04GW-Q100
+1V1
R228 8.25K
+1V1_ADC P29
R243 22K
GND
VBOOST_5V
R230 DNP
115K
VBOOST_ADC P29
R247 22K DNP
12V Load Switch
P12V
R837 0
VBAT_12V
R838 0
U81
VIN
VOUT
CT
EN/UVLO
QOD
GND
EPAD
TPS22810DRVT
P12_SWOUT
R840 0
P12V_SW
C1680 1uF
R839 0
C1681 0.1uF
P3_3V_LDO3
C1682 4700pf
BUCK1/2_0V8
P0_8V
R823 0
R824 0
R825 0
R826 0
LDO1_1V8
R816 0
P1_8V_ANA
P1_8V_IO
R812 0
P1_8V_ANA
P1_8V_IO_QSPI
P1_8V_IO_QSPI
R809 0
VDD_IO_QSPI
P3_3V_STBY_BRD
R808 0
P3_3V_STBY_MCU
LDO2_1V8
R815 0
P1_8V_IO
HVLDO_0V8
R811 0
P0_8V_STBY
P3_3V_IO3P3
R810 0
VDD_IO_USB
BUCK3_1V1
P1_1V
R821 0
R822 0
LDO3_3V3
P3_3V_IO3P3
R814 0
R813 0
P3_3V_LDO3
P12V_SW
J50
HDR 1X3
DNP
FAN
VPRE_3V3
P3_3V
R818 0
R819 0
R820 0
For Peripheral
P3_3V_STBY_BRD
R817 0
For S32G
BH2 MH_126
BH1 MH_126
BH5 MH_126
BH6 MH_126
BH3 MH_126
BH4 MH_126
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Classification: Company Internal/Proprietary
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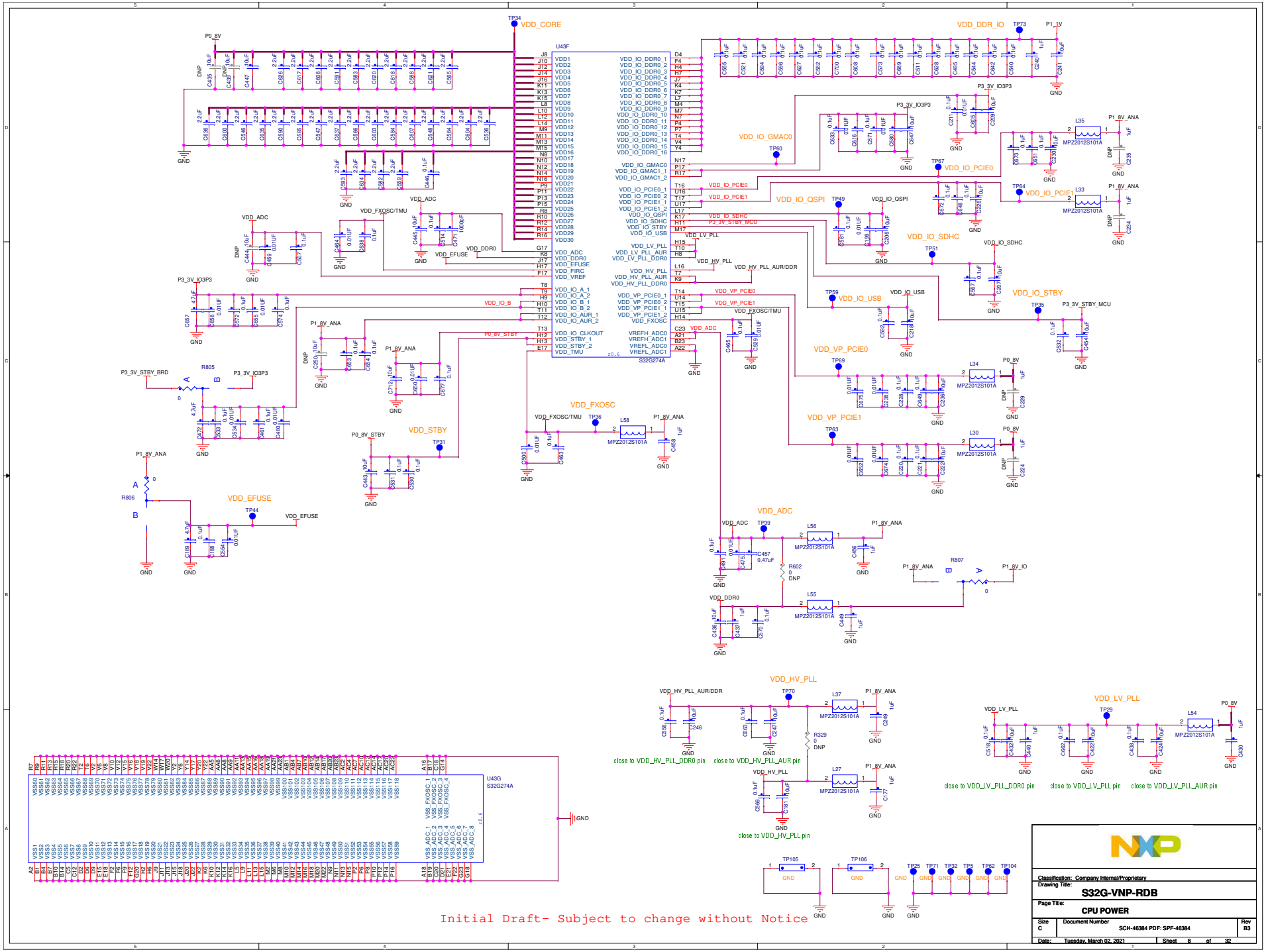
VDD_CORE
VDD_DDR_IO
VDD_IO_GMAC0
VDD_IO_PCIE0
VDD_IO_PCIE1
VDD_IO_QSPI
VDD_IO_SDHC
VDD_IO_USB
VDD_IO_STBY
VDD_VP_PCIE0
VDD_VP_PCIE1
VDD_ADC
VDD_FXOSC
VDD_STBY
VDD_EFUSE
VDD_HV_PLL
VDD_LV_PLL
U43F
U43G
S32G274A
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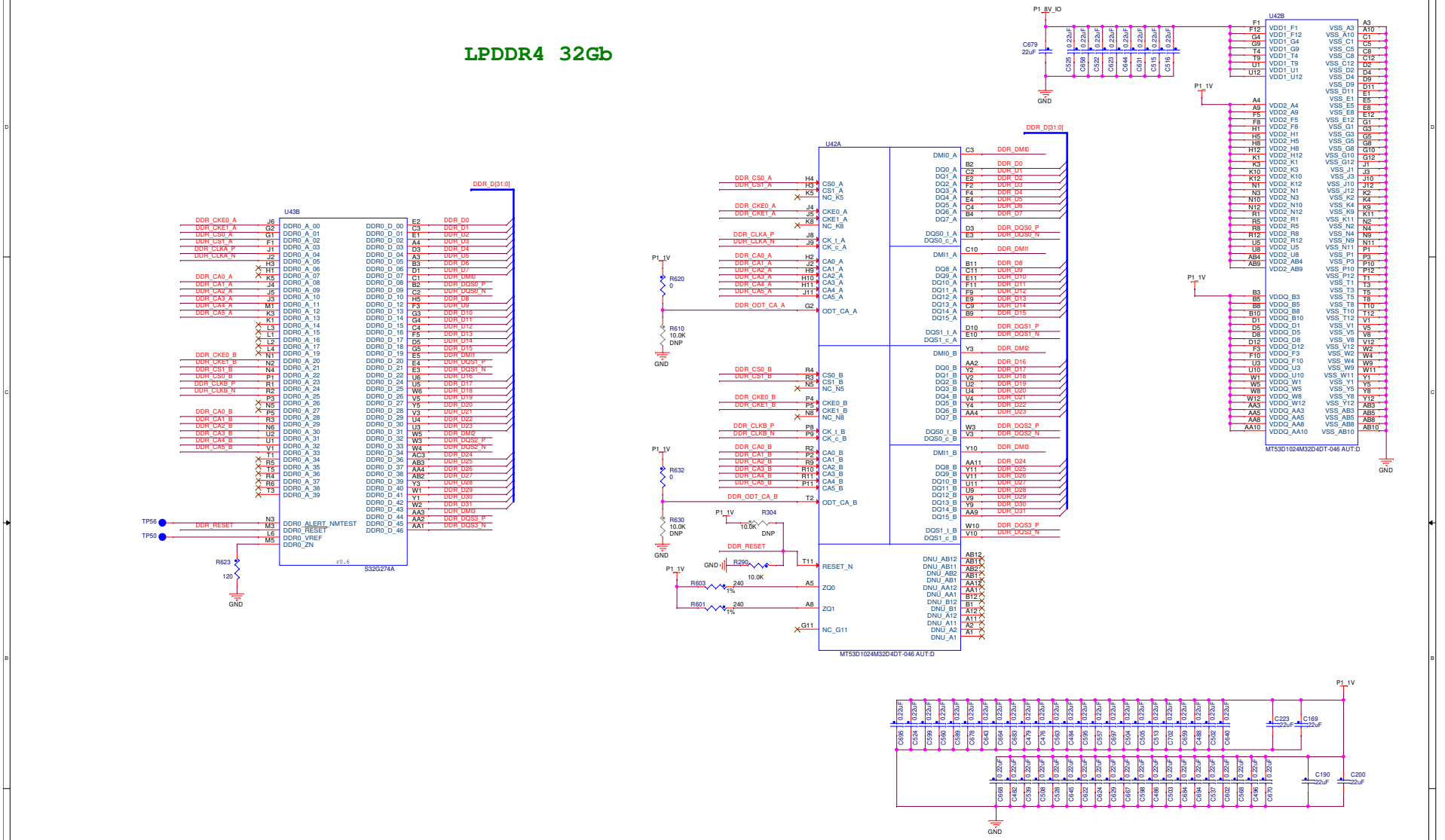
LPDDR4 32Gb



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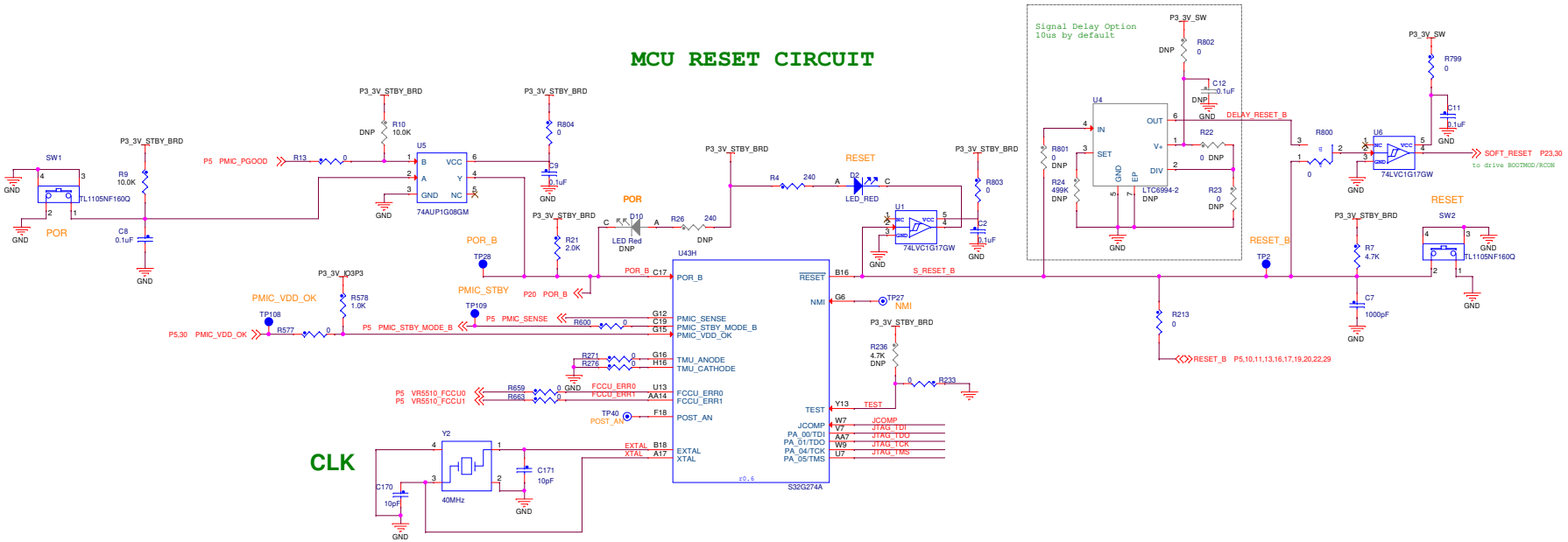
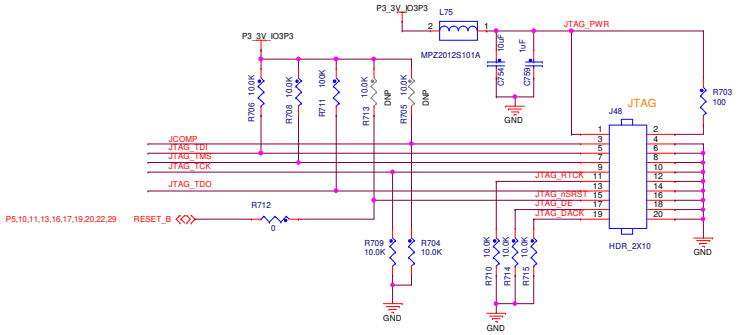
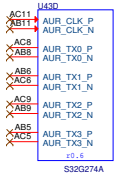
MCU RESET CIRCUIT



CLK

20-Pin JTAG





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Page Title:	RESET/CLOCK/JTAG
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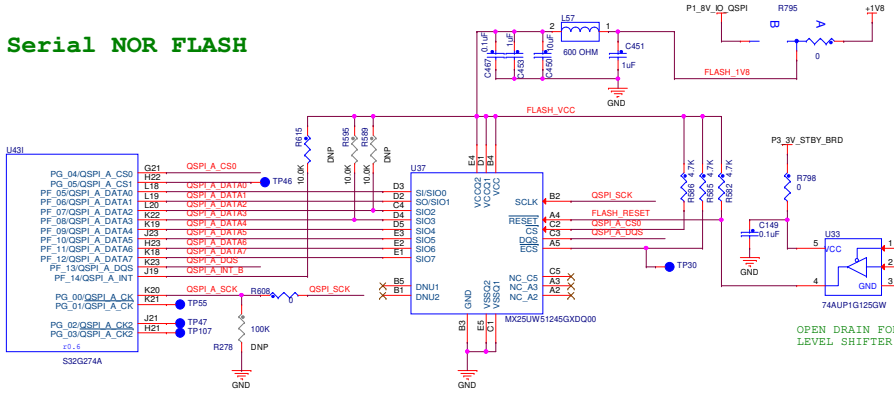
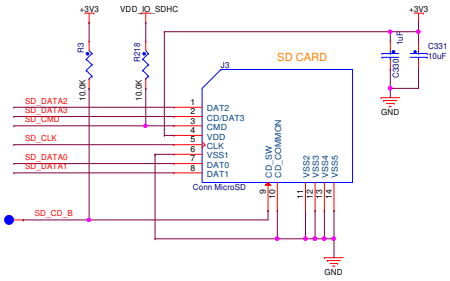
Serial NOR FLASH

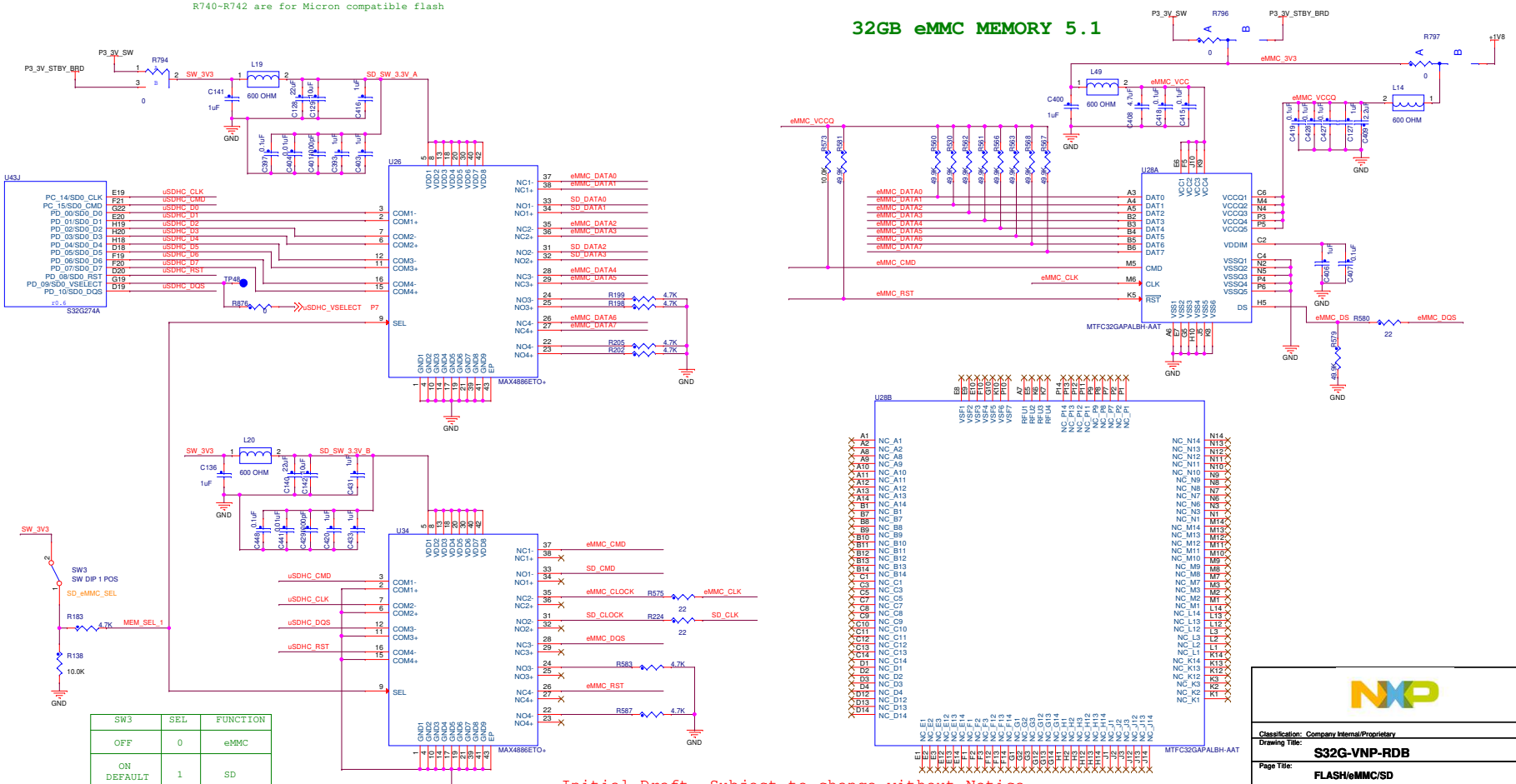


R740~R742 are for Micron compatible flash

MICRO SD CARD SOCKET



32GB eMMC MEMORY 5.1



SW3	SEL	FUNCTION
OFF	0	eMMC
ON DEFAULT	1	SD

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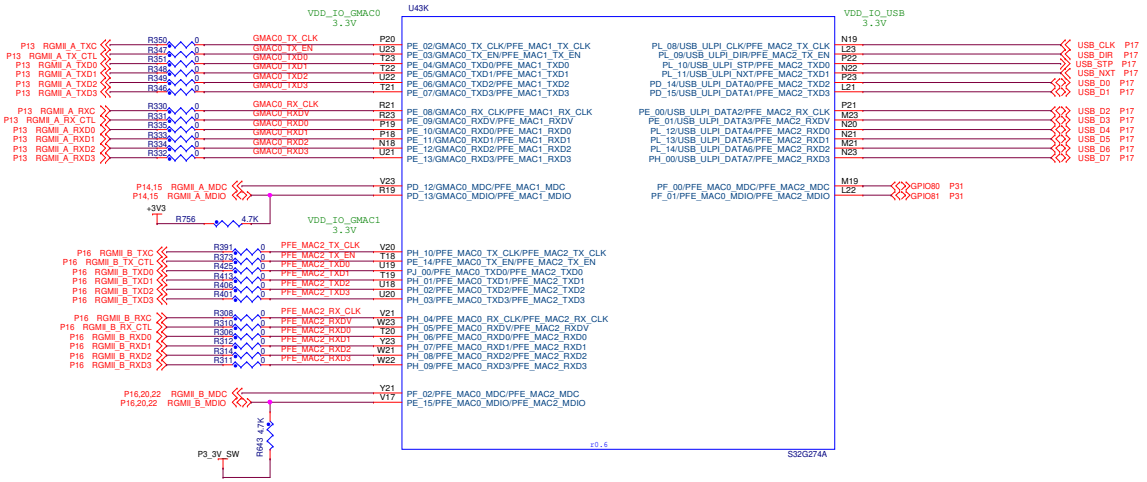

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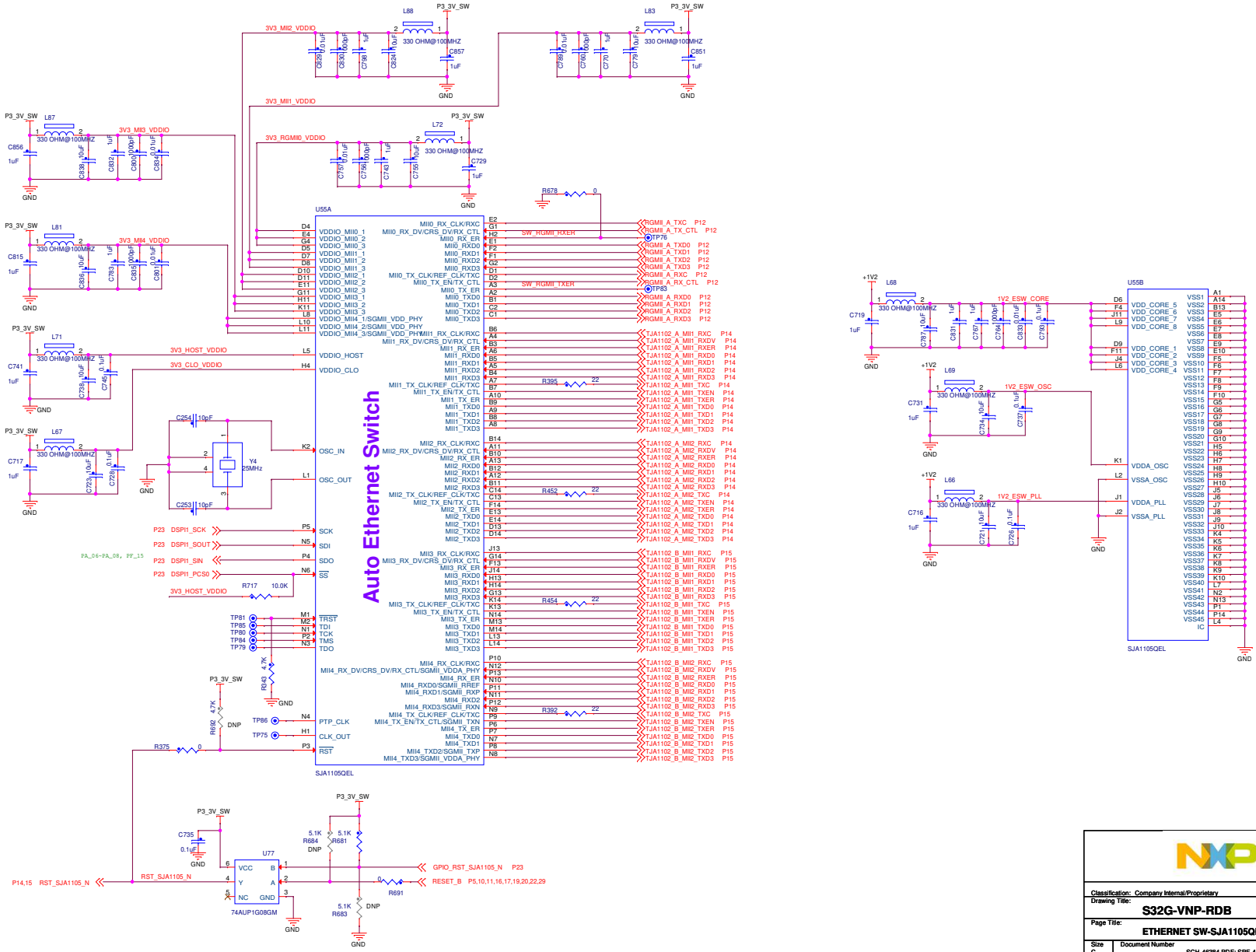

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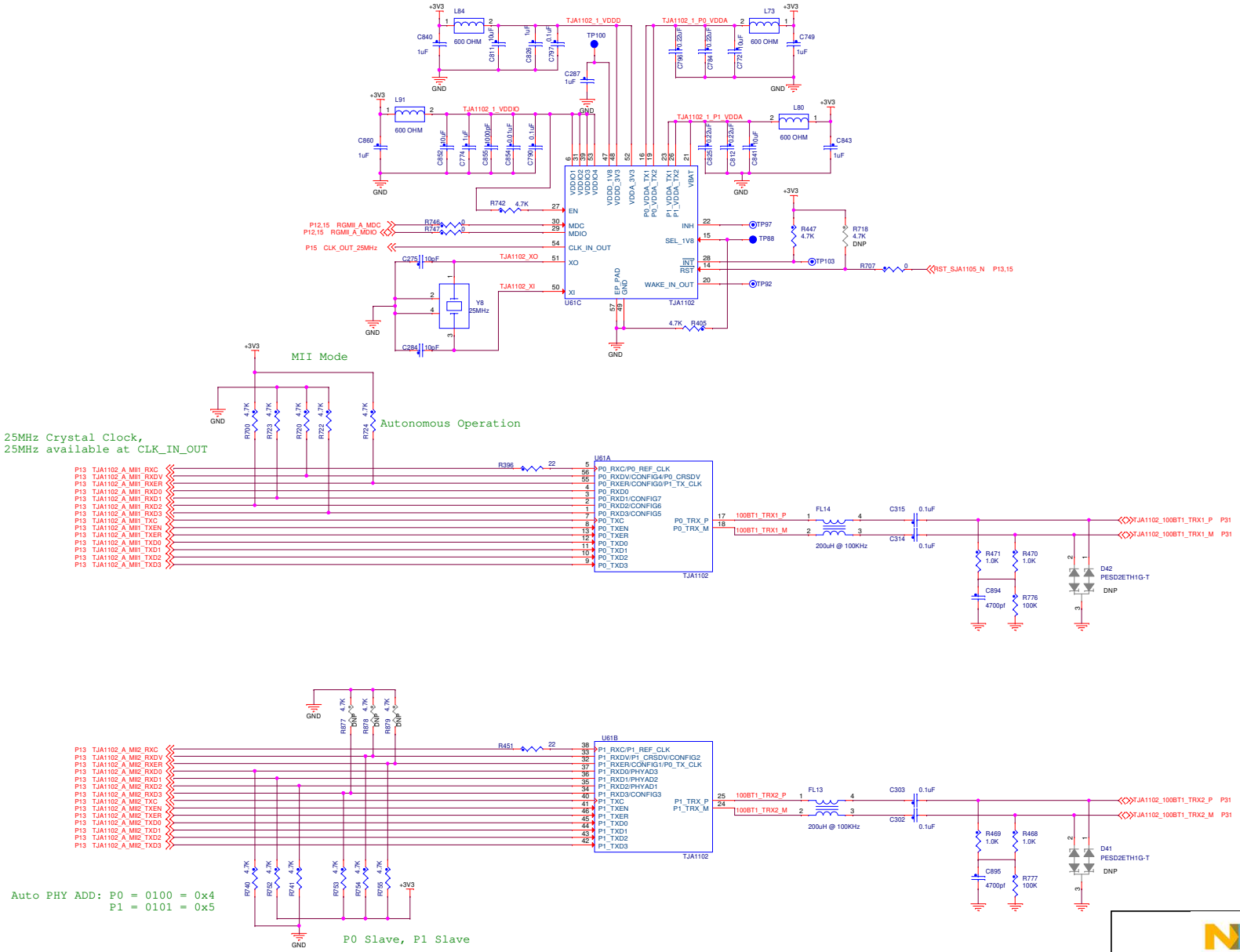

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Page Title: **DUAL PHY TJA1102_1**

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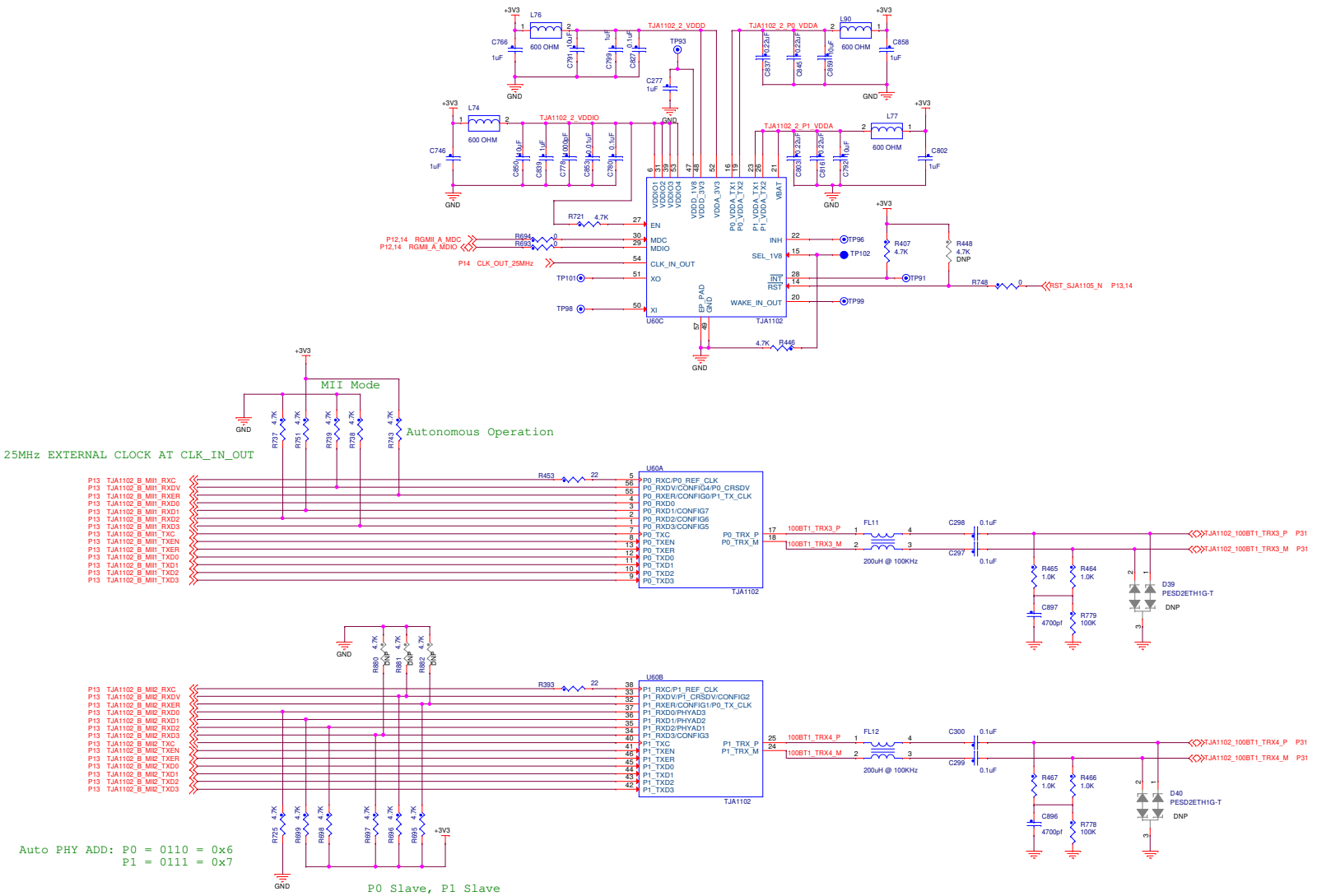

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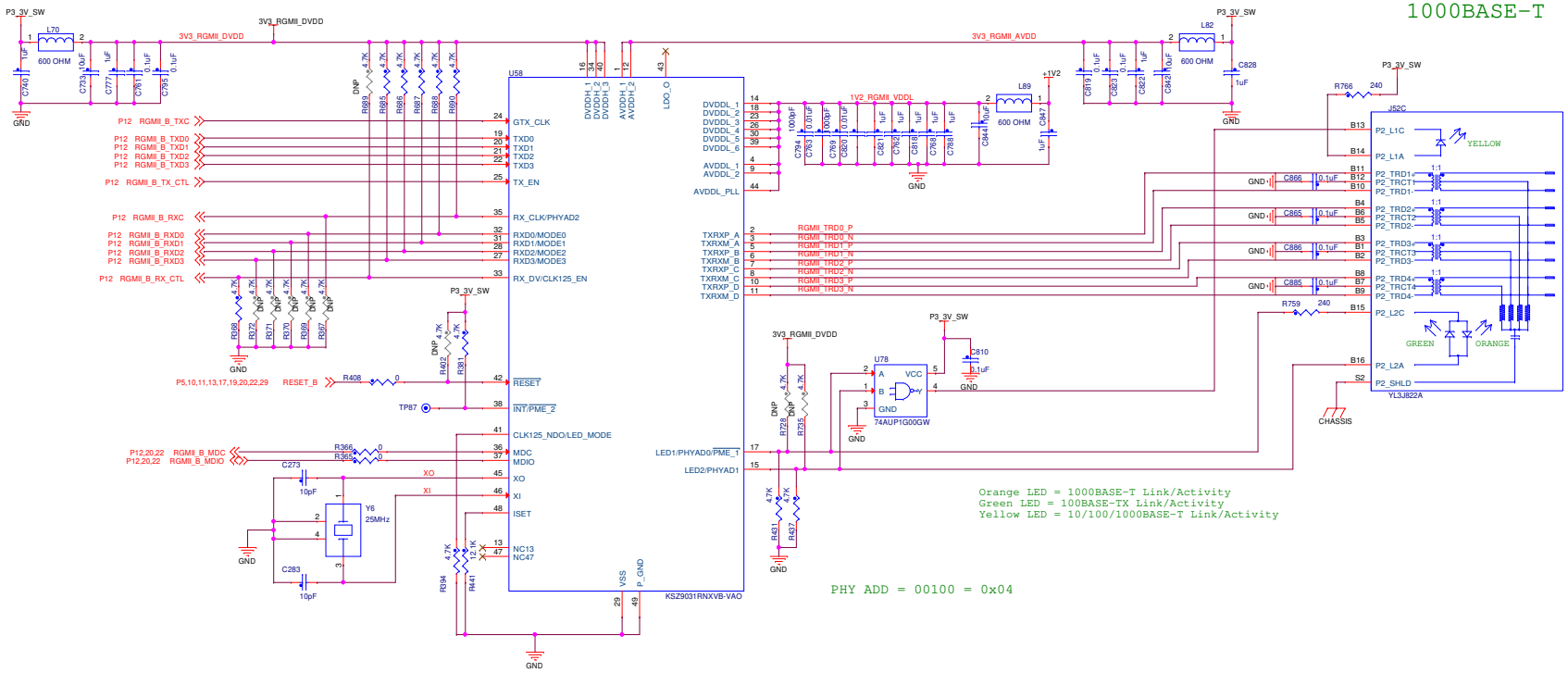

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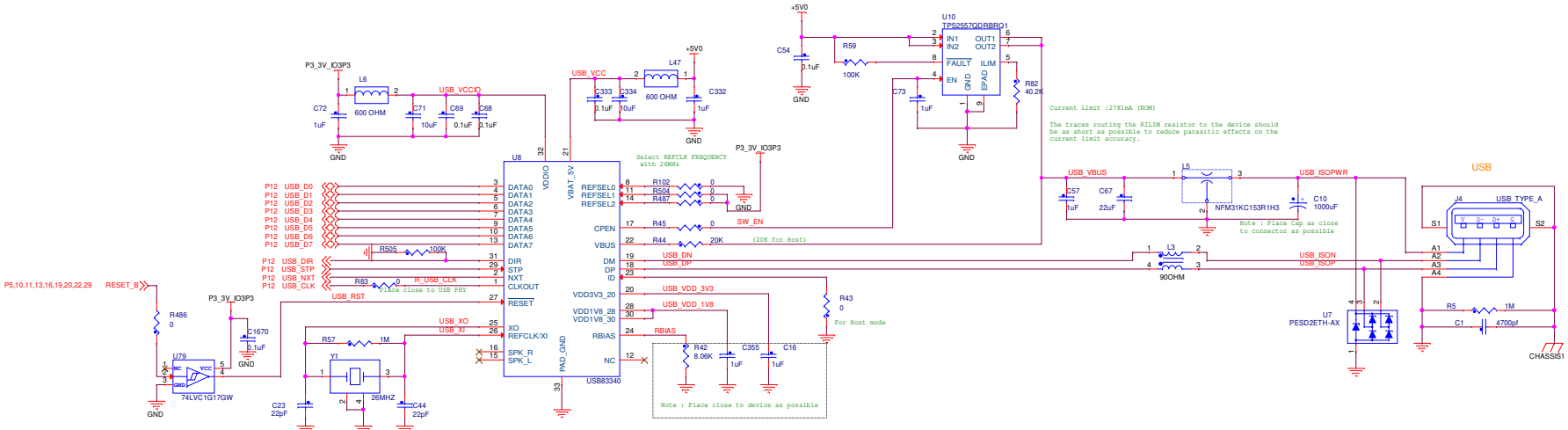

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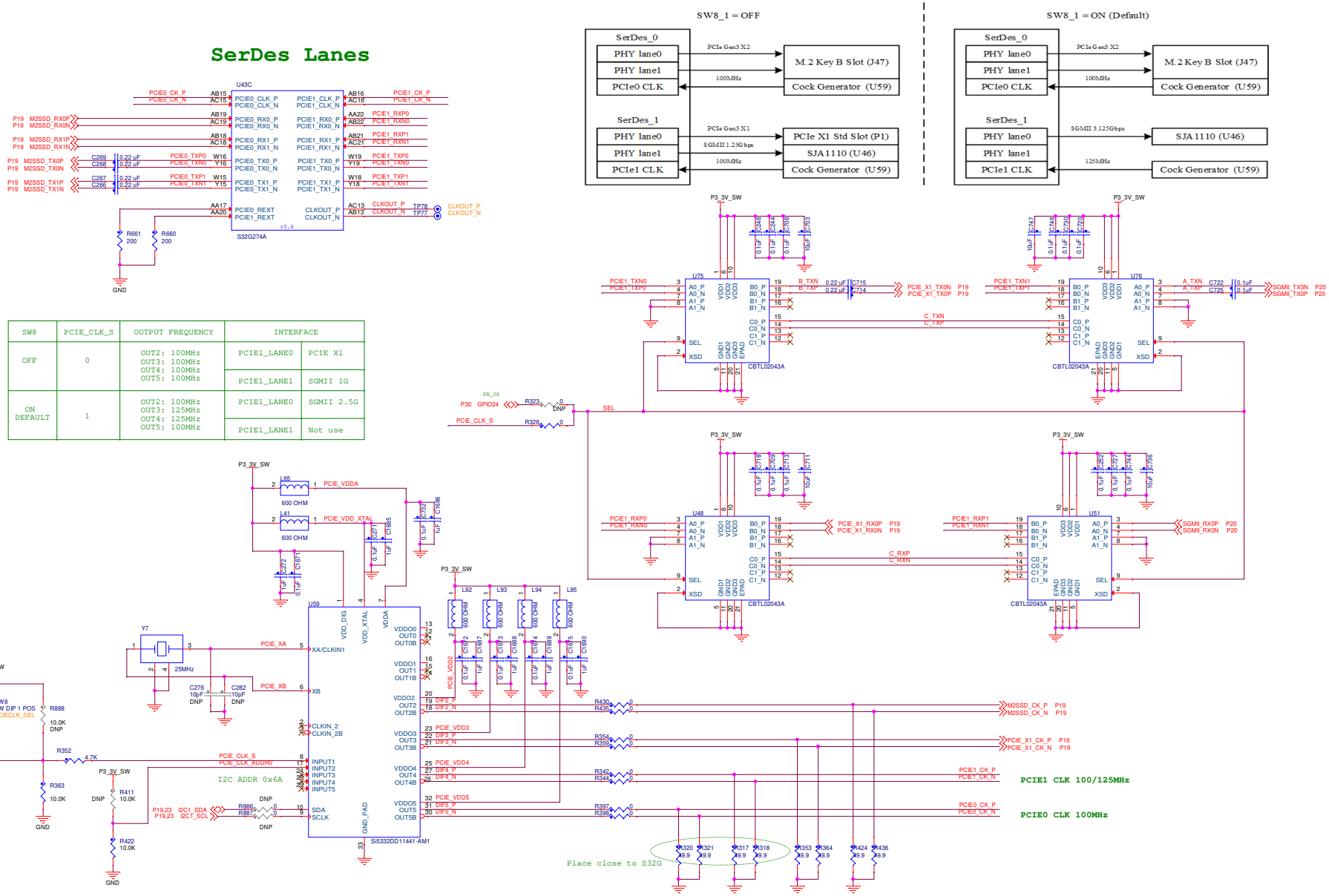
SerDes Lanes



SW8	PCIE_CLK_S	OUTPUT FREQUENCY	INTERFACE	
OFF	0	OUT2: 100MHz OUT3: 100MHz OUT4: 100MHz OUT5: 100MHz	PCIE1_LANE0	PCIE X1
			PCIE1_LANE1	SGMII 1G
ON DEFAULT	1	OUT2: 100MHz OUT3: 125MHz OUT4: 125MHz OUT5: 100MHz	PCIE1_LANE0	SGMII 2.5G
			PCIE1_LANE1	Not use

NXP

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Page Title: **PCIECLK/SERDES**

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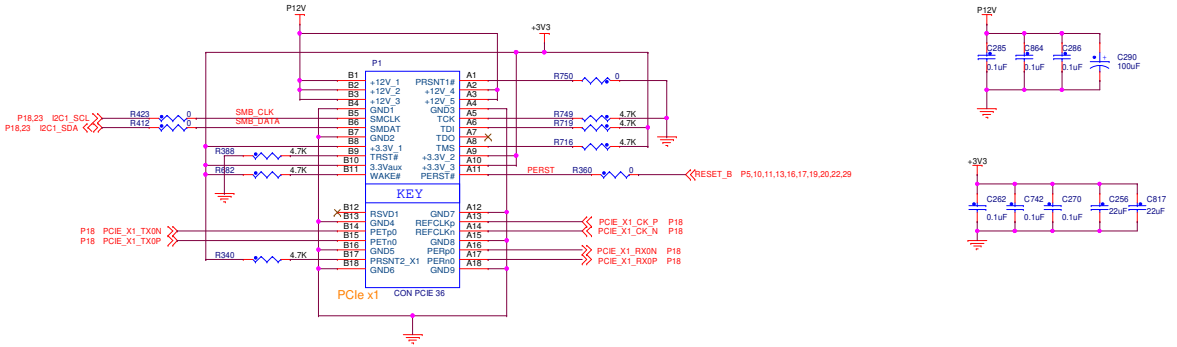
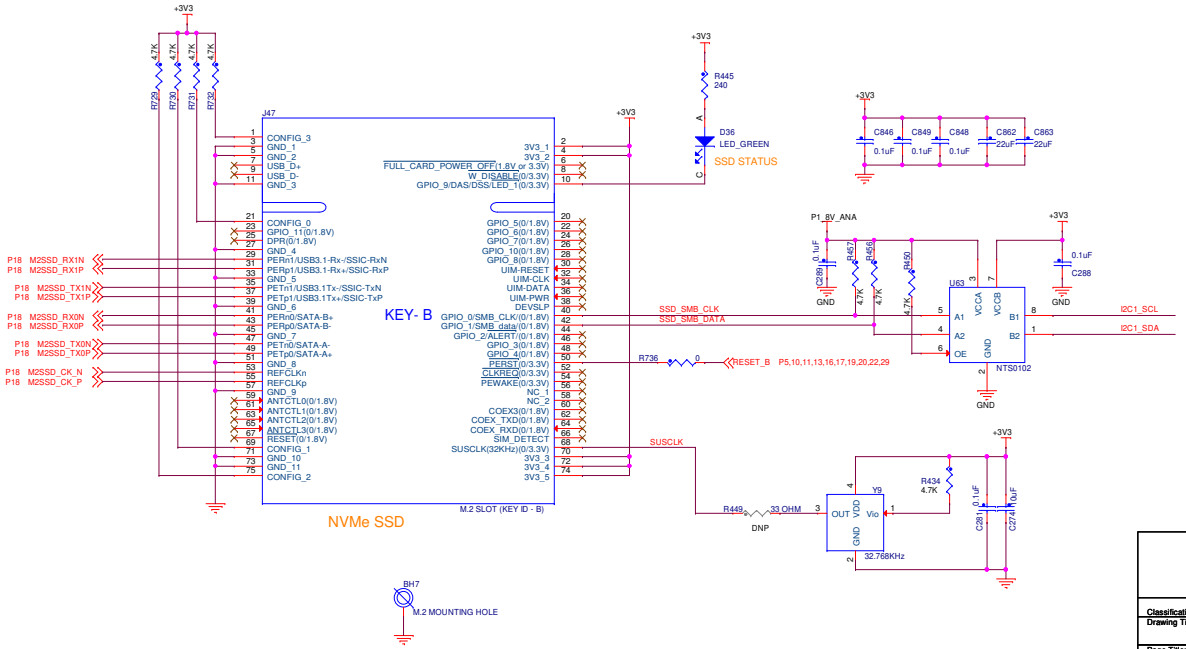
PCIe X1 Connector



M.2 Connector (Socket 2)
PCIe x2 SSD 2242 (Type B)



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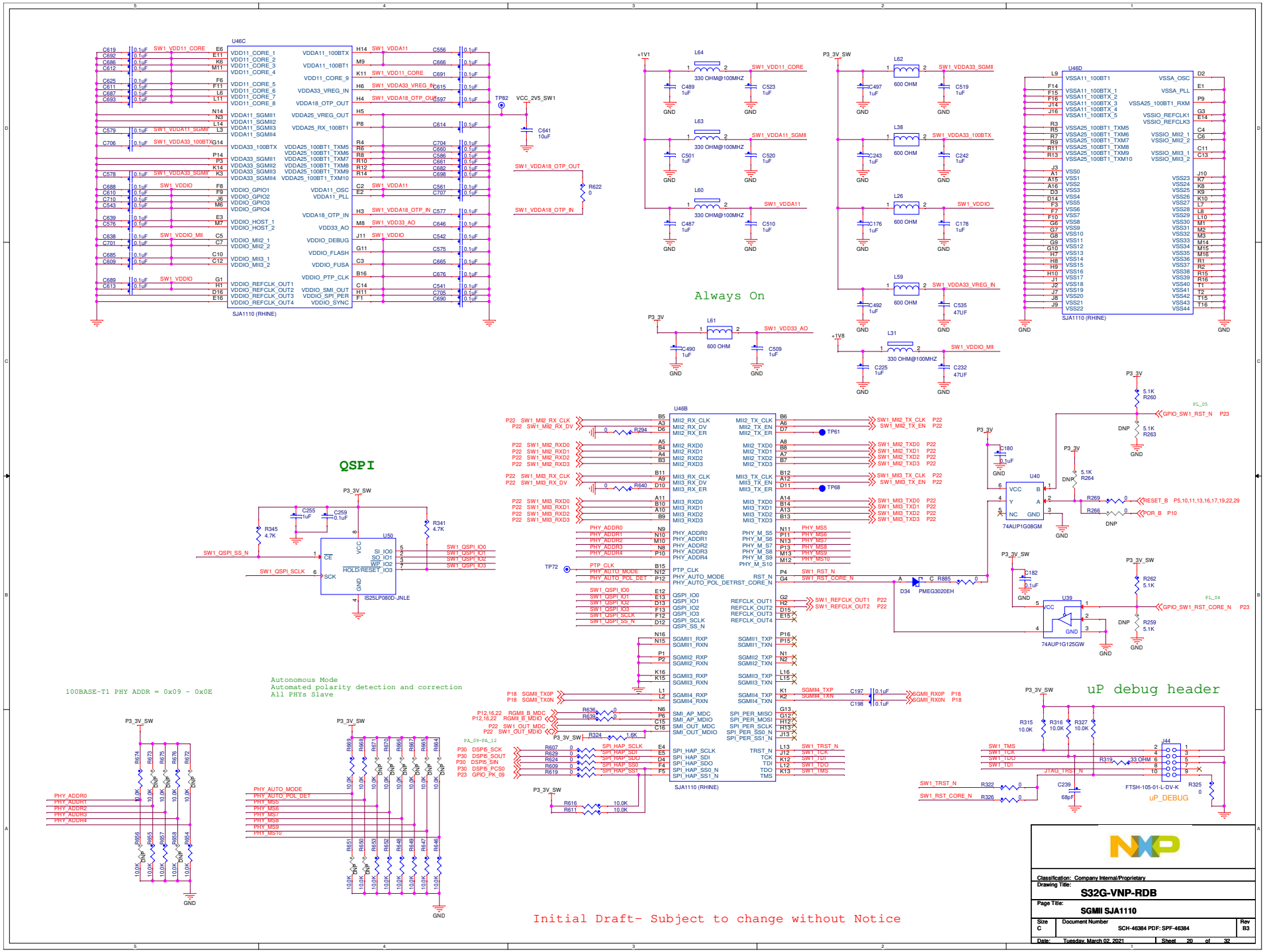
U46C
SJA1110 (RHINE)
SW1_VDD11_CORE
SW1_VDDA33_100BTX
SW1_VDDA33_SGMII
SW1_VDDIO
SW1_VDDIO_MII
SW1_VDDA11_SGMII
SW1_VDDA18_OTP_OUT
SW1_VDDA18_OTP_IN
SW1_VDDA11
SW1_VDD33_AO
SW1_VDDA33_VREG_IN
VCC_2V5_SW1
TP82
R622
U46D
U46B
Always On
QSPI
P3_3V_SW
+1V1
+1V8
P3_3V
GND
U50
IS25LP080D-JNLE
SW1_QSPI_SS_N
SW1_QSPI_SCLK
SW1_QSPI_IO0
SW1_QSPI_IO1
SW1_QSPI_IO2
SW1_QSPI_IO3
U40
74AUP1G08GM
U39
74AUP1G125GW
D34
PMEG3020EH
TP61
TP68
TP72
RESET_B
POR_B
GPIO_SW1_RST_N
GPIO_SW1_RST_CORE_N
100BASE-T1 PHY ADDR = 0x09 ~ 0x0E
Autonomous Mode
Automated polarity detection and correction
All PHYs Slave
uP debug header
uP_DEBUG
FTSH-105-01-L-DV-K
Initial Draft- Subject to change without Notice
Classification: Company Internal/Proprietary
Drawing Title:
S32G-VNP-RDB
Page Title:
SGMII SJA1110
Size C
Document Number
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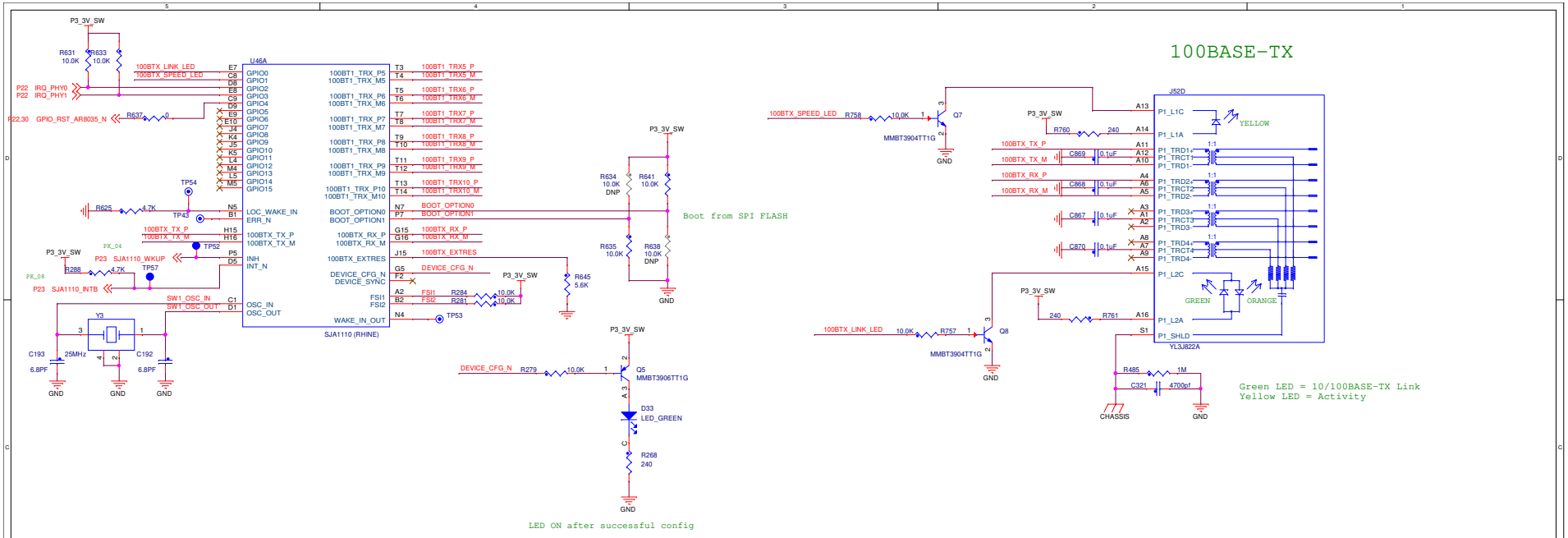

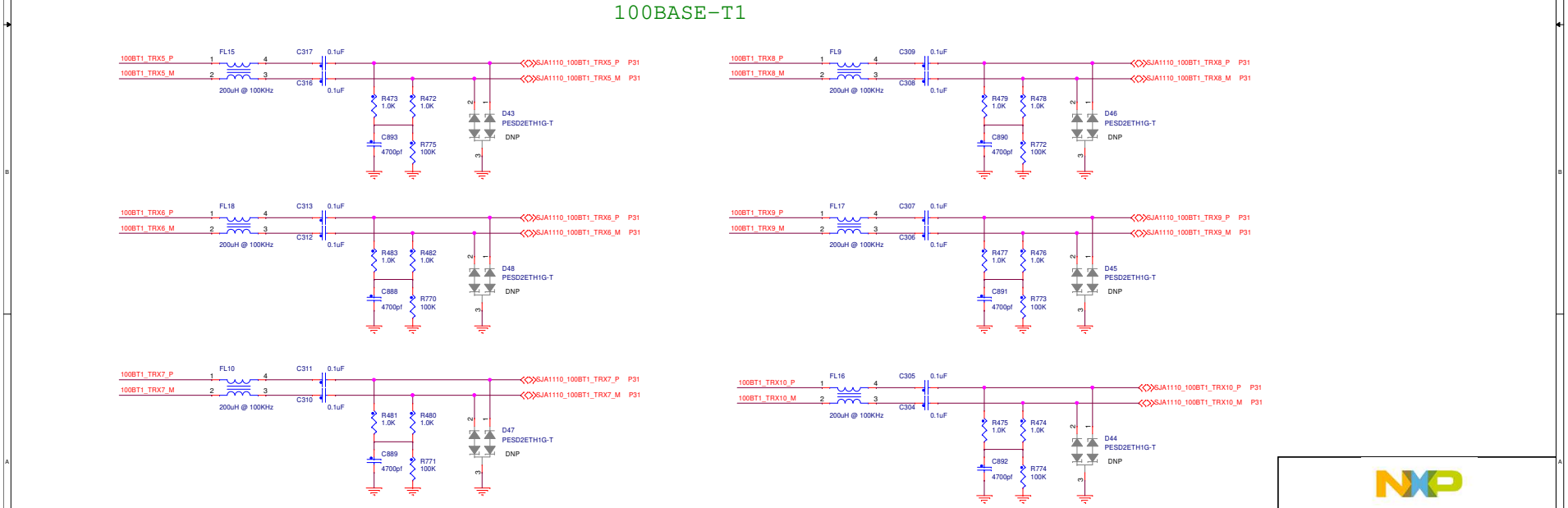

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Classification:	Company Internal/Proprietary
Drawing Title:	S32G-VNP-RDB
Page Title:	SGMII SJA1110 100BASE-T1/TX
Size: C	Document Number: SCH-46384 PDF: SPF-46384
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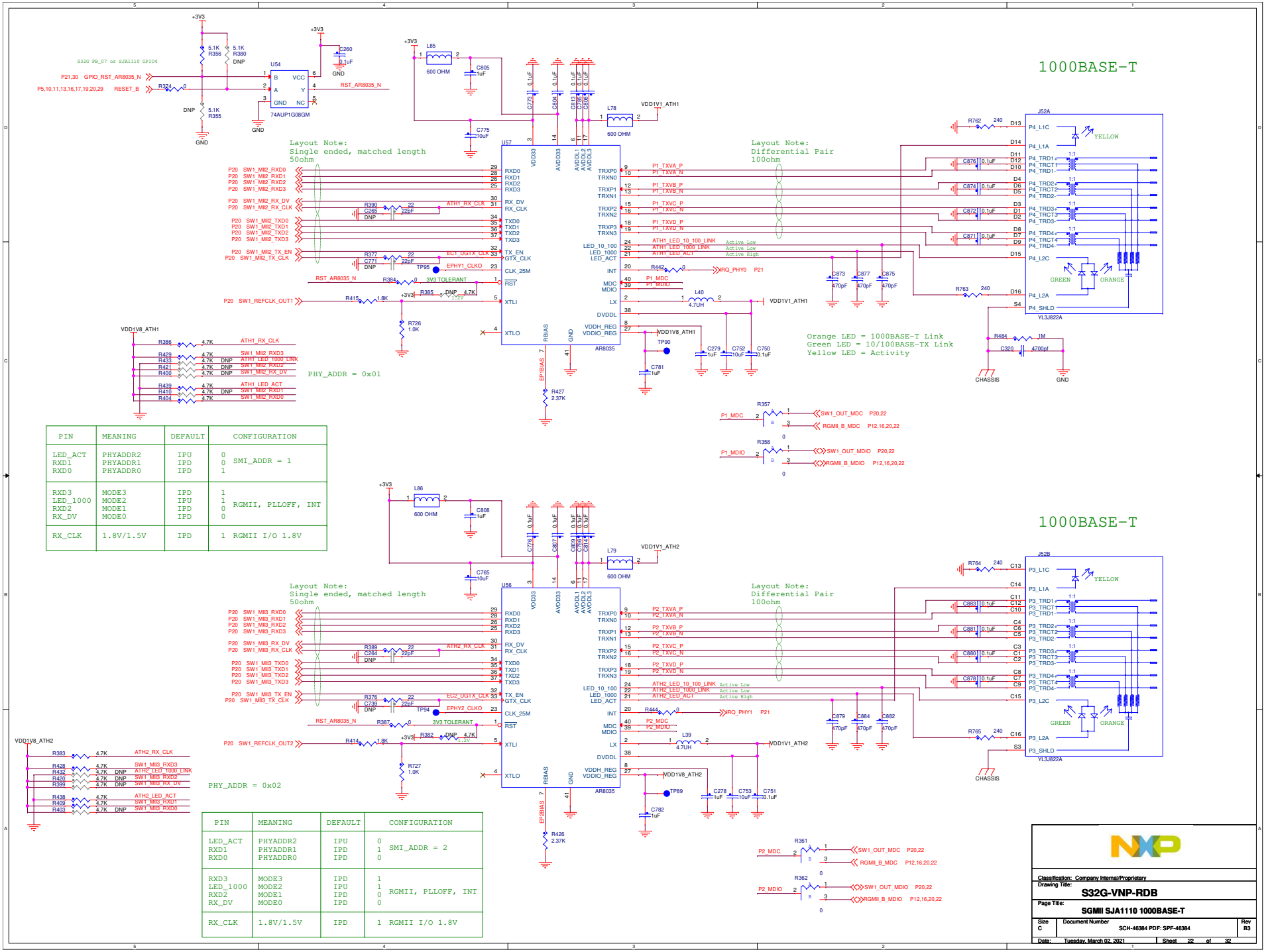

PIN	MEANING	DEFAULT	CONFIGURATION
LED_ACT	PHYADDR2	IPU	0
RXD1	PHYADDR1	IPD	0 SMI_ADDR = 1
RXD0	PHYADDR0	IPD	1
RXD3	MODE3	IPD	1
LED_1000	MODE2	IPU	1 RGMII, PLLOFF, INT
RXD2	MODE1	IPD	0
RX_DV	MODE0	IPD	0
RX_CLK	1.8V/1.5V	IPD	1 RGMII I/O 1.8V

PIN	MEANING	DEFAULT	CONFIGURATION
LED_ACT	PHYADDR2	IPU	0
RXD1	PHYADDR1	IPD	1 SMI_ADDR = 2
RXD0	PHYADDR0	IPD	0
RXD3	MODE3	IPD	1
LED_1000	MODE2	IPU	1 RGMII, PLLOFF, INT
RXD2	MODE1	IPD	0
RX_DV	MODE0	IPD	0
RX_CLK	1.8V/1.5V	IPD	1 RGMII I/O 1.8V

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Drawing Title: **S32G-VNP-RDB**

Page Title: **SGMII SJA1110 1000BASE-T**

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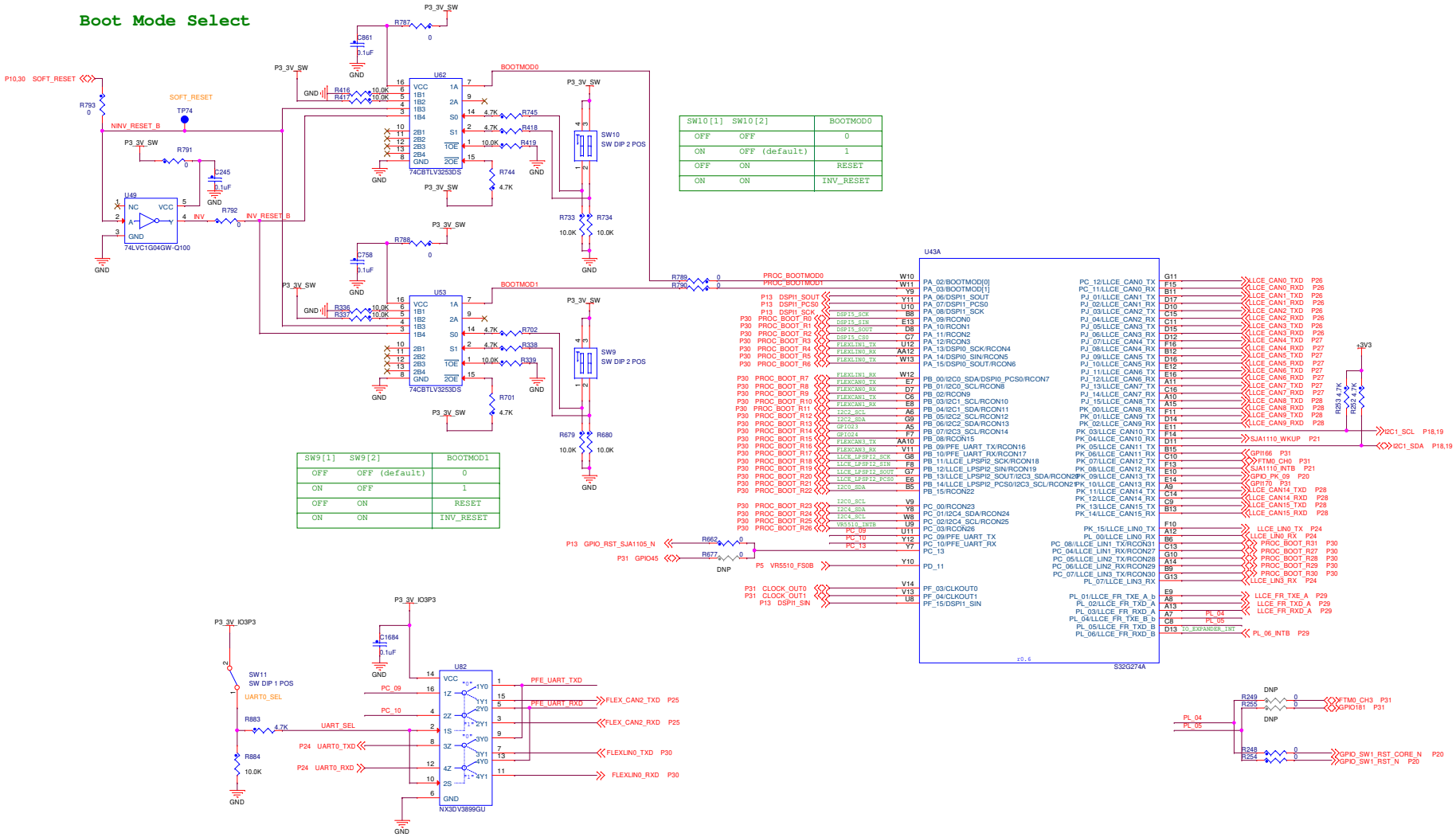
Boot Mode Select



SW10[1]	SW10[2]	BOOTMOD0
OFF	OFF	0
ON	OFF (default)	1
OFF	ON	RESET
ON	ON	INV_RESET

SW9[1]	SW9[2]	BOOTMOD1
OFF	OFF (default)	0
ON	OFF	1
OFF	ON	RESET
ON	ON	INV_RESET

SW11	SEL	FUNCTION
OFF DEFAULT	0	PC_09, PC_10 -> UART0 PORT
ON	1	PC_09, PC_10 -> FLEX_CAN2 FLEXLIN0 -> UART0 PORT

NXP

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Drawing Title: **S32G-VNP-RDB**

Page Title: **S32G PORT**

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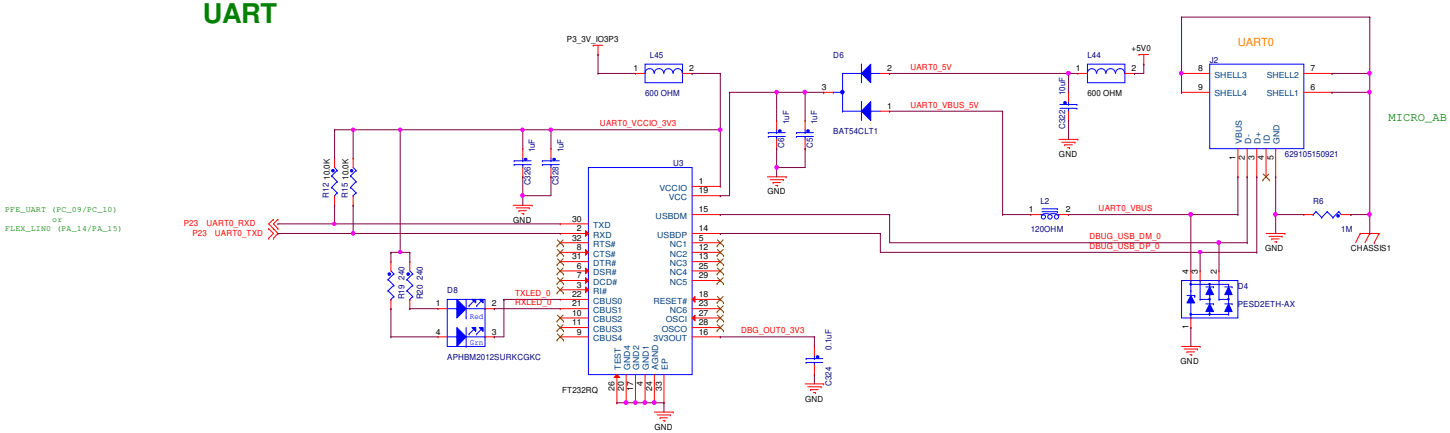
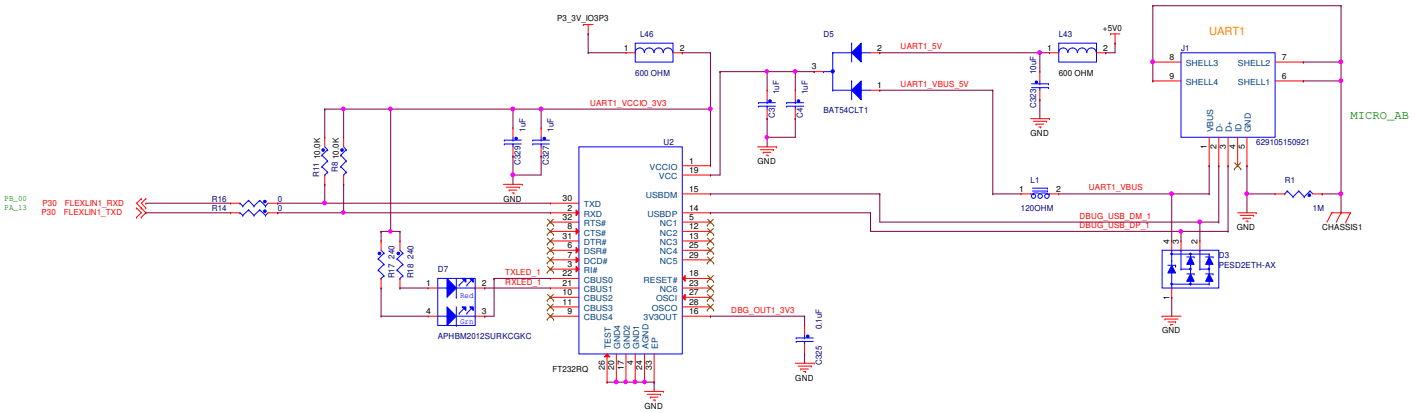
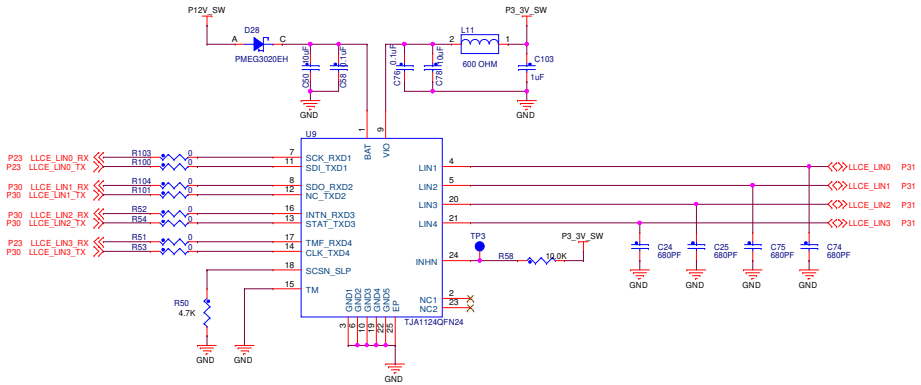
UART





LIN



Classification: Company Internal/Proprietary
Drawing Title: S32G-VNP-RDB
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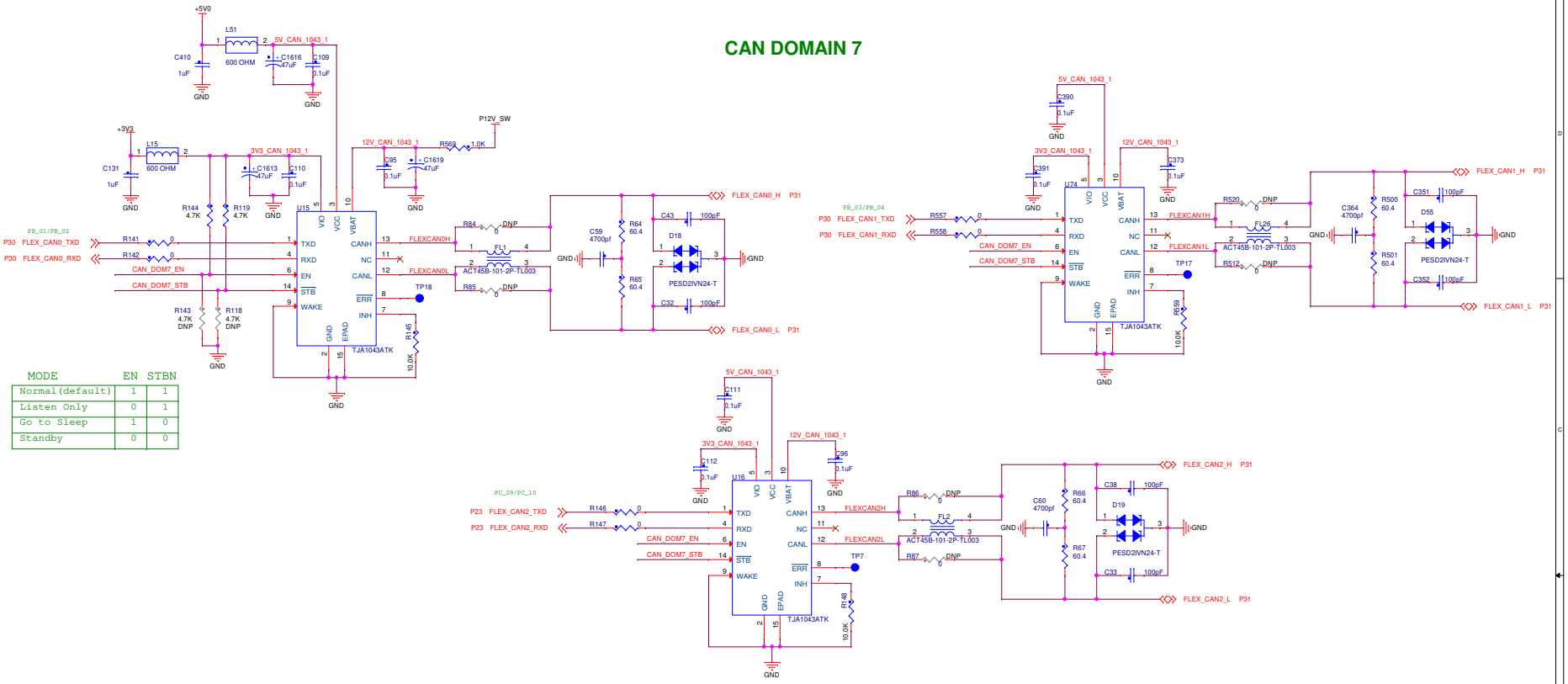
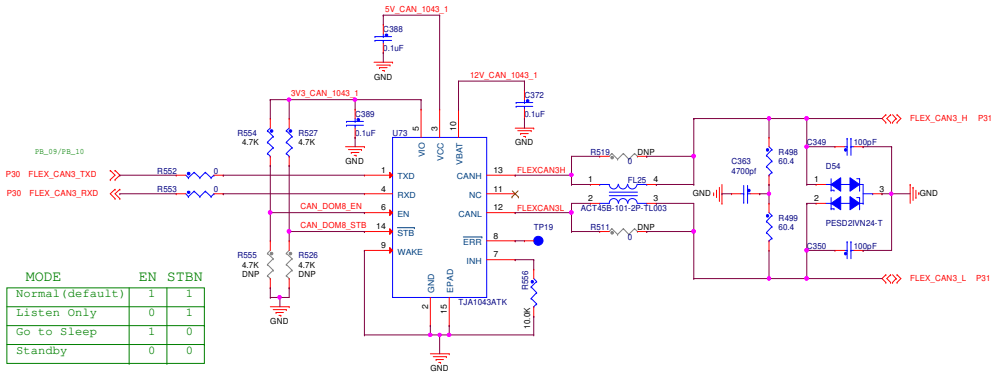
CAN DOMAIN 7



MODE	EN	STBN
Normal(default)	1	1
Listen Only	0	1
Go to Sleep	1	0
Standby	0	0

CAN DOMAIN 8



MODE	EN	STBN
Normal(default)	1	1
Listen Only	0	1
Go to Sleep	1	0
Standby	0	0

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Drawing Title: S32G-VNP-RDB

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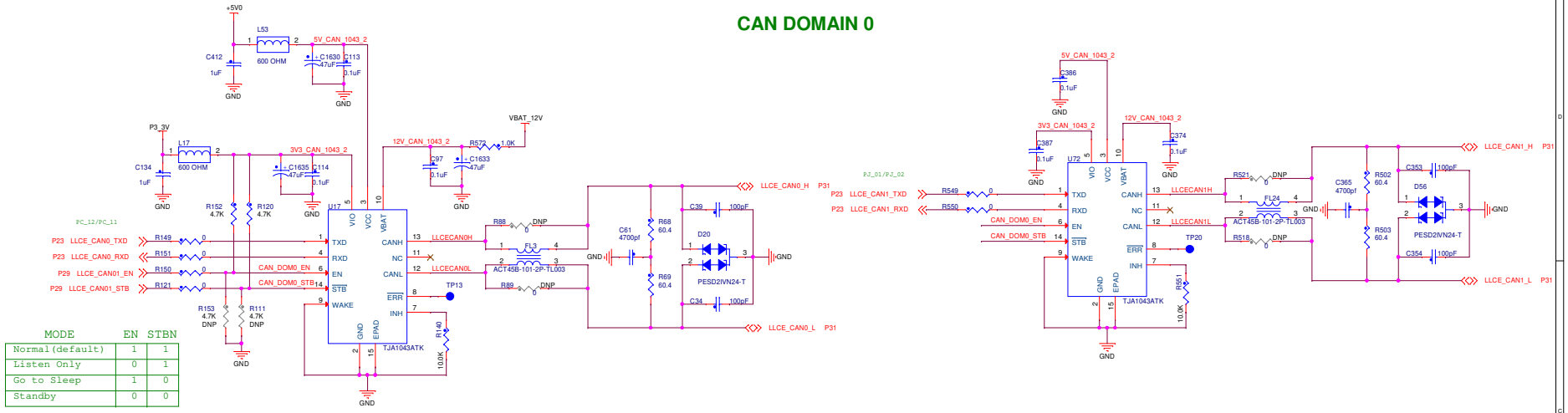
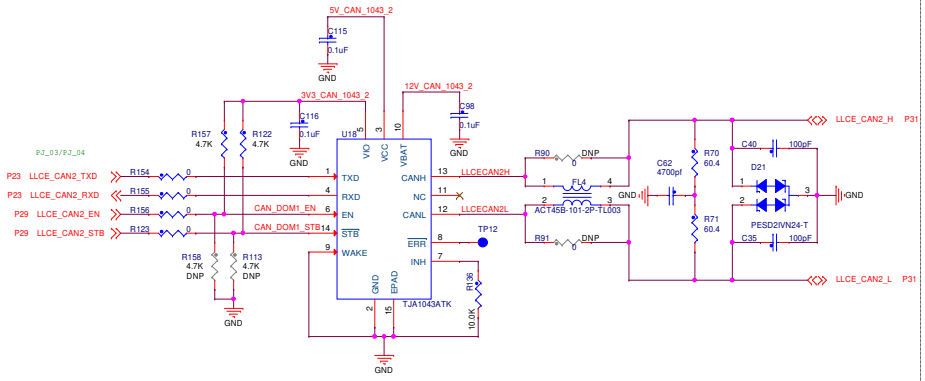
CAN DOMAIN 0



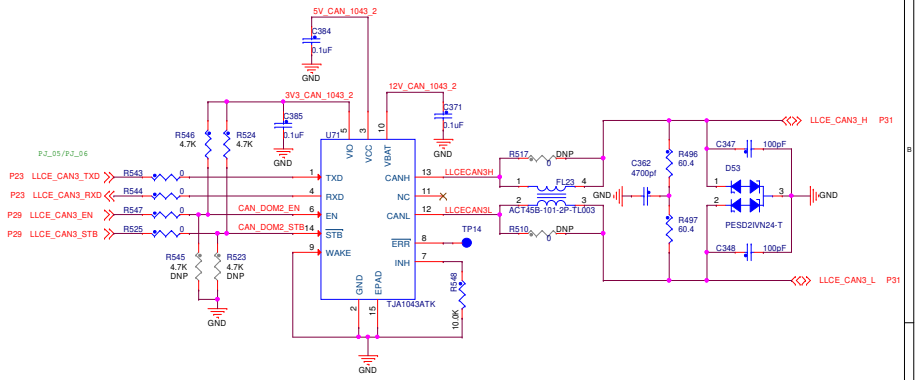
MODE	EN	STBN
Normal(default)	1	1
Listen Only	0	1
Go to Sleep	1	0
Standby	0	0

CAN DOMAIN 1



MODE	EN	STBN
Normal(default)	1	1
Listen Only	0	1
Go to Sleep	1	0
Standby	0	0

CAN DOMAIN 2



MODE	EN	STBN
Normal(default)	1	1
Listen Only	0	1
Go to Sleep	1	0
Standby	0	0

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Drawing Title: **S32G-VNP-RDB**

Page Title: **CAN TJA1043ATK_2**

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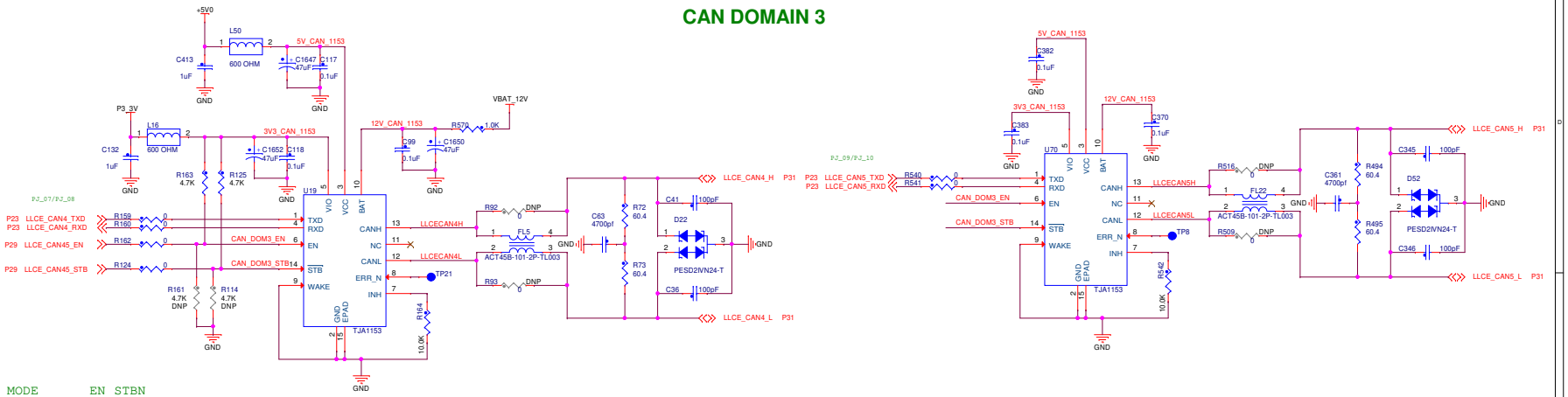
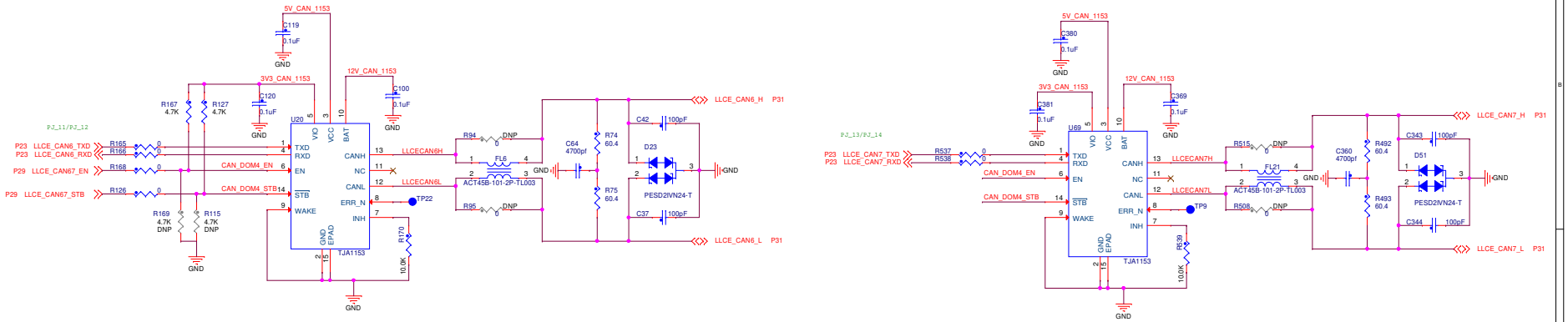
CAN DOMAIN 3



MODE	EN	STBN
Normal(default)	1	1
Listen Only	0	1
Go to Sleep	1	0
Standby	0	0

CAN DOMAIN 4



MODE	EN	STBN
Normal(default)	1	1
Listen Only	0	1
Go to Sleep	1	0
Standby	0	0

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Drawing Title: **S32G-VNP-RDB**

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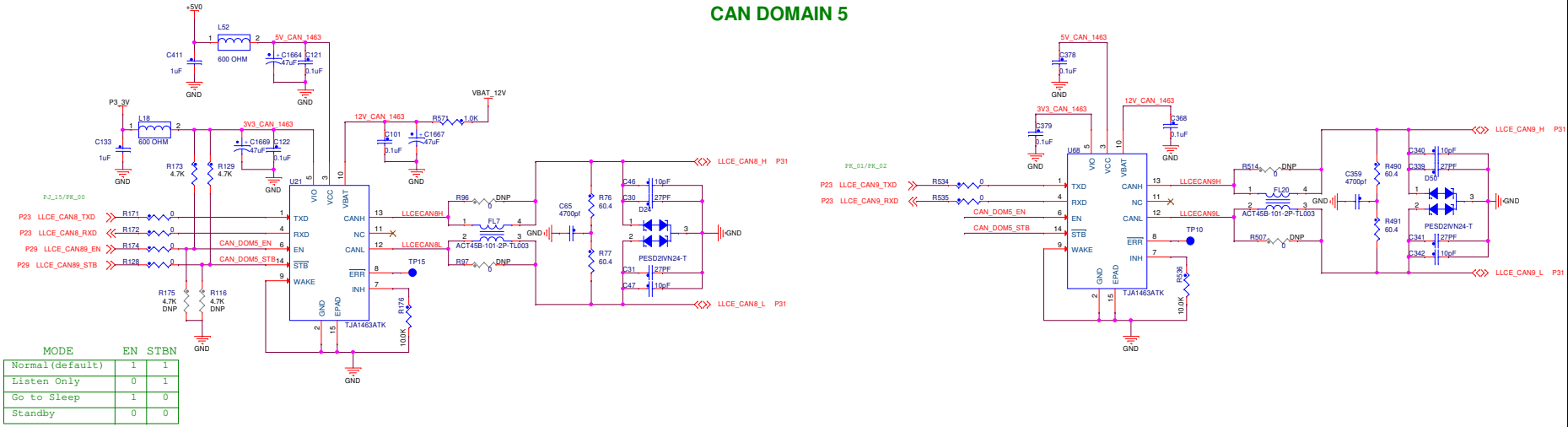
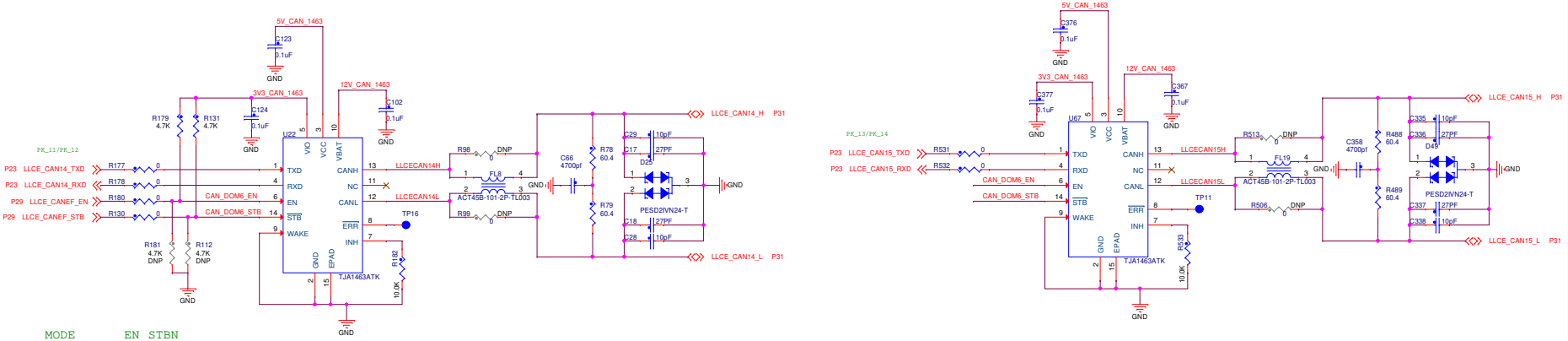
CAN DOMAIN 5



MODE	EN	STBN
Normal(default)	1	1
Listen Only	0	1
Go to Sleep	1	0
Standby	0	0

CAN DOMAIN 6



MODE	EN	STBN
Normal(default)	1	1
Listen Only	0	1
Go to Sleep	1	0
Standby	0	0

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Drawing Title: **S32G-VNP-RDB**

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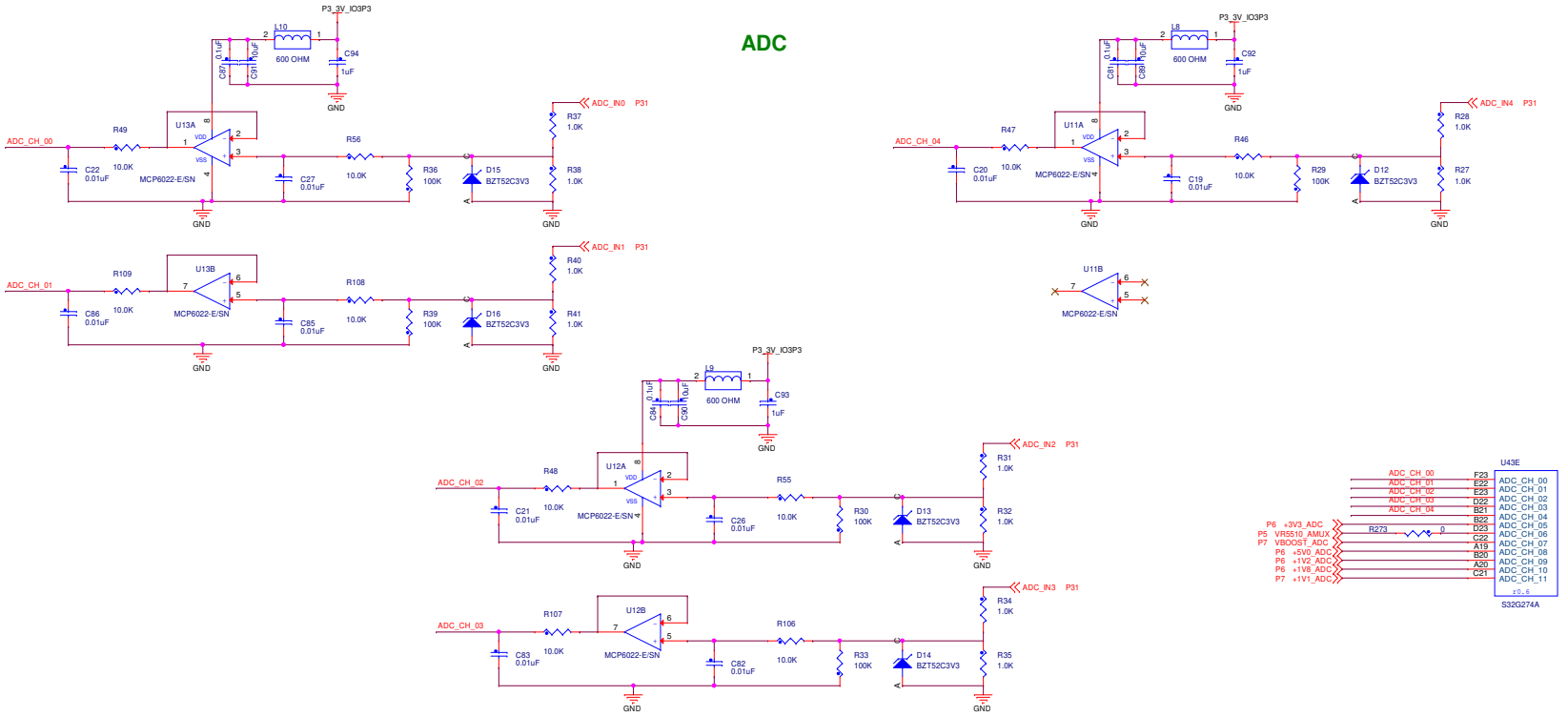
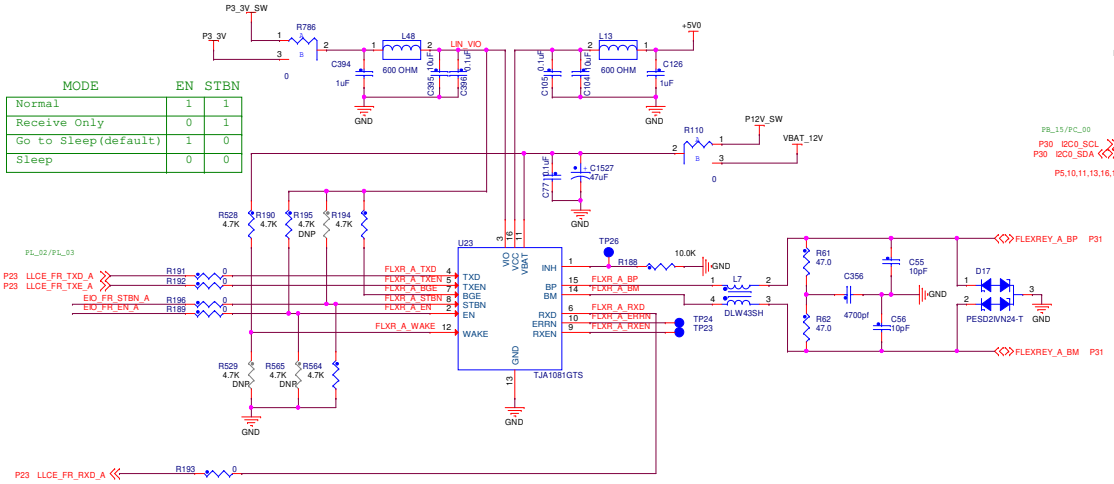
ADC

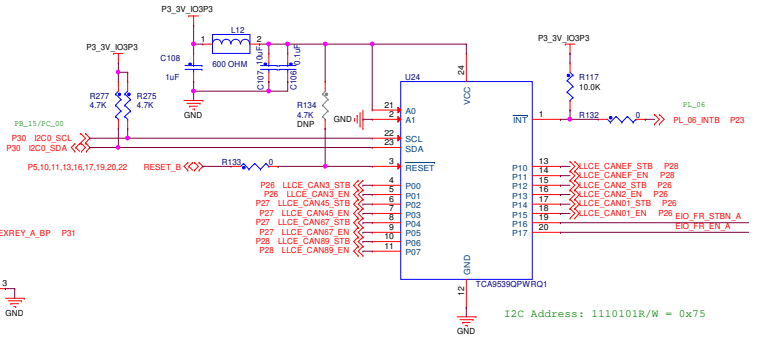


FLEXRAY



MODE	EN	STBN
Normal	1	1
Receive Only	0	1
Go to Sleep(default)	1	0
Sleep	0	0

IO EXPANDER



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Drawing Title: **S32G-VNP-RDB**

Page Title: **FLEXRAY/ADC/EXPAND_IO**

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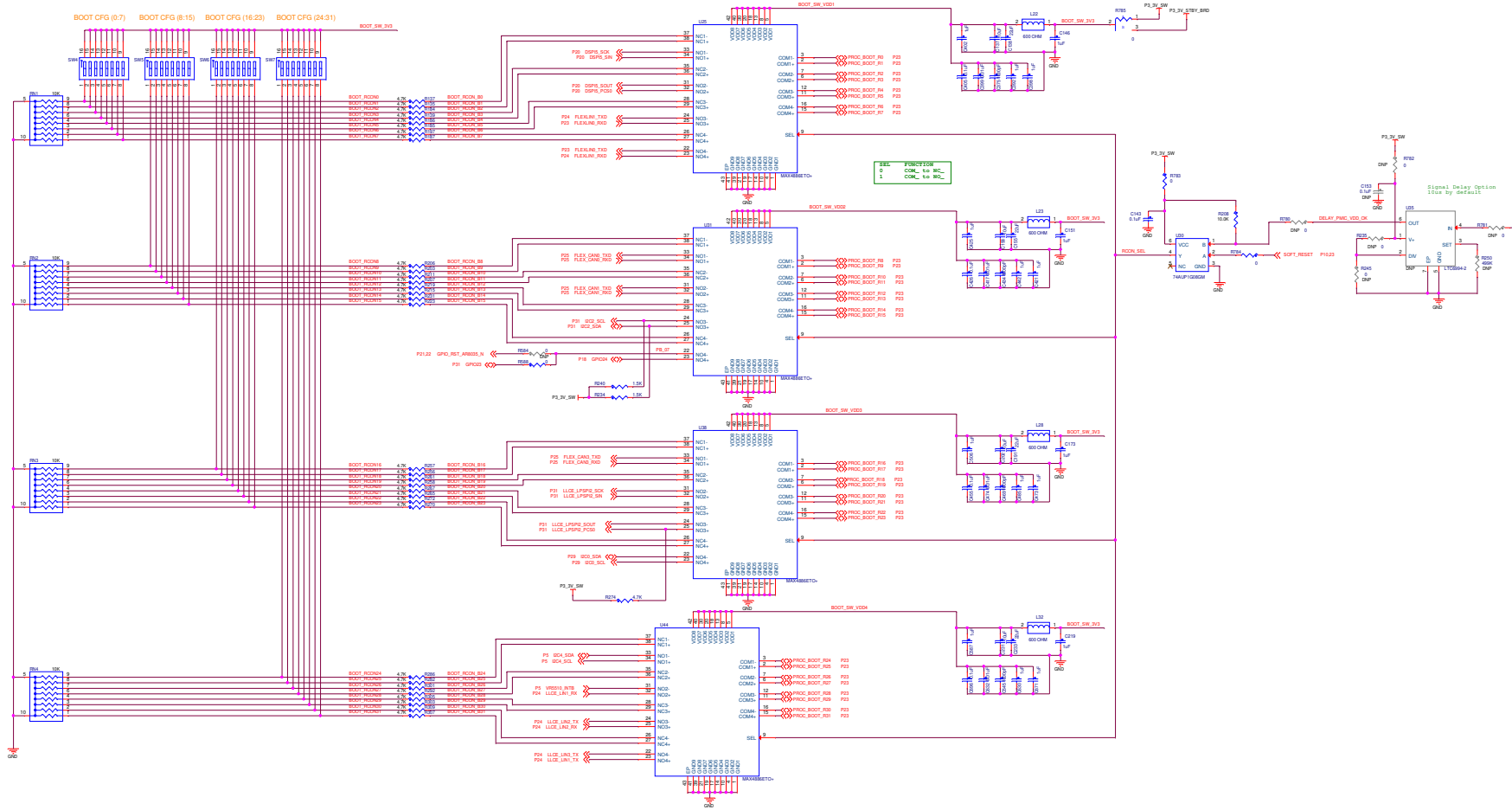
RCON Boot Selection

SW4~SW7 Default Setting

	1	2	3	4	5	6	7	8
SW4	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
SW5	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
SW6	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
SW7	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF



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Page Title:	RCON BOOT SELECT
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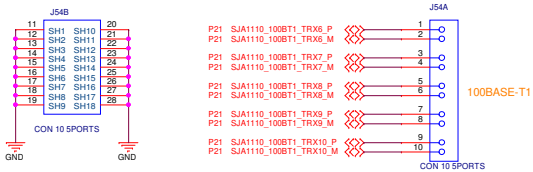

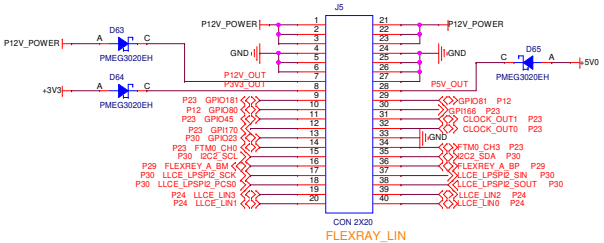

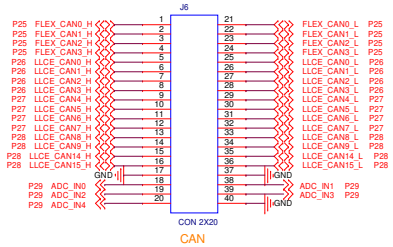

J5 GPIO Configuration Description

S32G Port		Multiplex function			Default function select	Note
PL_05	VDD_IO_B	GPIO181	R255 DNP	J5-PIN9		DNP R254 and populate R255 to enable this pin
		GPIO_SW1_RST_N	R254 populate	U46 (SJA1110)	✓	
PF_00	VDD_IO_USB	GPIO80		J5-PIN10	✓	Can be used as FTM1_CH5
PC_13	VDD_IO_A	GPIO45	R677 DNP	J5-PIN11		DNP R662 and populate R677 to enable this pin
		GPIO_RST_SJA1105_N	R662 populate	U55 (SJA1105)	✓	
PK_10	VDD_IO_STBY	GPI170		J5-PIN12	✓	
PB_07	VDD_IO_B	GPIO23	R588 populate	J5-PIN13	✓	
		RCON14			✓	
		GPIO_RST_AR8035_N	R584 DNP	U56 (AR8035) U57 (AR8035)		
PK_07	VDD_IO_B	FTM0_CH0		J5-PIN14	✓	
PB_05	VDD_IO_B	I2C2_SCL		J5-PIN15	✓	
		RCON12			✓	
PB_11	VDD_IO_B	LLCE_LPSPI2_SCK		J5-PIN17	✓	
		RCON18			✓	
PB_14	VDD_IO_B	LLCE_LPSPI2_PCS0		J5-PIN18	✓	
		RCON21			✓	
PF_01	VDD_IO_USB	GPIO81		J5-PIN29	✓	
PK_06	VDD_IO_STBY	GPI166		J5-PIN30	✓	Input only, can be used as wakeup source WKUP11
PF_04	VDD_IO_CLKOUT	GPIO84		J5-PIN31	✓	1.8V GPIO, can be used as Clock Output
PF_03	VDD_IO_CLKOUT	GPIO83		J5-PIN32	✓	1.8V GPIO, can be used as Clock Output
PL_04	VDD_IO_B	FTM0_CH3	R249 DNP	J5-PIN34		DNP R248 and populate R249 to enable this pin
		GPIO_SW1_RST_CORE_N	R248 populate	U4 (SJA1110)	✓	
PB_06	VDD_IO_B	I2C2_SDA		J5-PIN35	✓	
		RCON13			✓	
PB_12	VDD_IO_B	LLCE_LPSPI2_SIN		J5-PIN37	✓	
		RCON19			✓	
PB_13	VDD_IO_B	LLCE_LPSPI2_SOUT		J5-PIN38	✓	
		RCON20			✓	

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Default Jumper setting:

REF DES	JUMPER(DEFAULT)	PAGE NAME
R866,R868	A	05 POWER VR5510
R210,R460	A	06 POWER DCDC_1
R812,R204	A	07 POWER DCDC_2
R807,R805,R806	A	08 CPU POWER
R800	A	10 RESET/CLOCK/JTAG
R794,R796,R795,R797	A	11 FLASH/eMMC/SD
R358,R361,R362,R357	A	22 SGMII SJA1110 1000BASE-T
R110,R786	A	29 FLEXRAY/ADC/EXPAND_IO
R785	A	30 RCON BOOT

Default Switch setting:

REF DES	SWITCH(DEFAULT)	PAGE NAME
SW3	ON	11 FLASH/eMMC/SD
SW8	ON	18 PCIECLK/SERDES
SW9	1-OFF, 2-OFF	23 S32G PORT
SW10	1-ON, 2-OFF	23 S32G PORT
SW11	OFF	23 S32G PORT
SW7,SW6,SW5	1-OFF,2-OFF,3-OFF,4-OFF, 5-OFF,6-OFF,7-OFF,8-OFF	30 RCON BOOT
SW4	1-OFF,2-OFF,3-OFF,4-OFF, 5-OFF,6-OFF,7-ON,8-OFF	30 RCON BOOT

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Page Title: DEFAULT JUMPER SETTING

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