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LS1043A:
GVDD=1.35V
DDR_VTT & VREF=0.675V
OVDD=1.8V
EVDD=1.8V
DVDD=3.3V
VDD=1.025V
SVDD=1.025V
XVDD=1.35V
LVDD=1.8V
TVDD=1.8V
USB_SVDD & SDVDD=1.025V
USB_HVDD=3.3V
PROG_SFP=1.8/0V
PROG_MTR=0V

Rev	Date	Changes
X1	02 Jan,2018	A070 Release
A1	22 Feb,2019	A085 Release
AX1	13 May,2019	A070 Release for Rev-B design
B	22 May,2019	A085 Release

REV-B Changes:

1. Added pullup resistor R18 on CPU_HRESET_B signal.
2. Added level shifter ICs (U25, U26) to convert 1.8V level of LED drive signals on RGMII PHYs (U36, U37) to 3.3V level.
3. Reset supervisory circuit (U11) for MPC5748G is deleted.
4. Marked R493 as DNP. R492 is changed to be mounted.
5. R487 is changed to 0 ohm.
6. Added J6 for LS1043A heatsink fan supply
7. Added R35, R36. Marked R476 and R478 as DNP to indicate Rev-B PCB revision.
8. Replaced R49, R50 by two 1x2 headers (J18, J19).

MPC-LS-VNP-RDB

Digital Networking Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

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Drawn by: Debasis & Sumit	Page Title: TITLE		
Approved: Manav Marwah	Size C	Document Number SCH-45700 PDF: SPF-45700	Rev B
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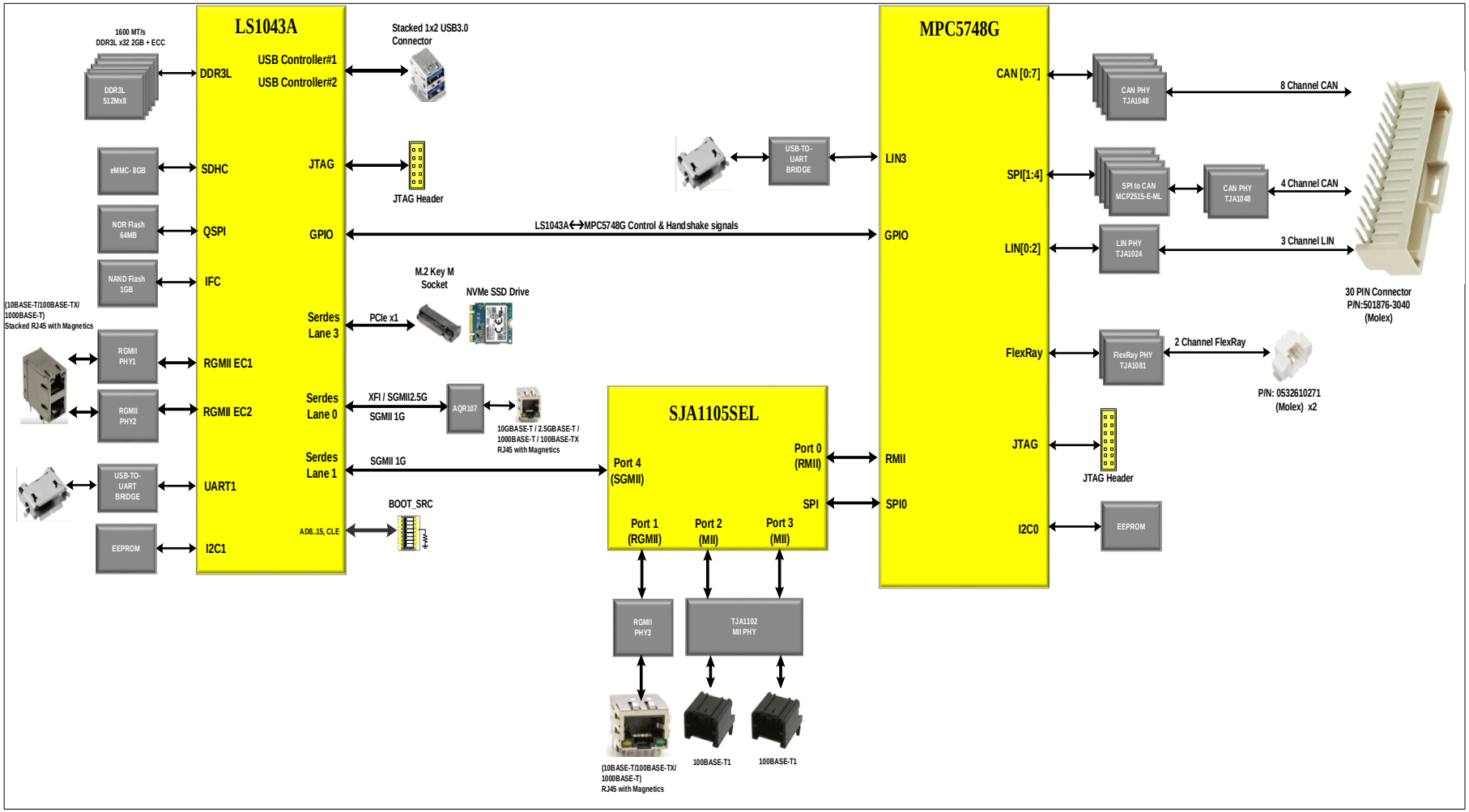
BLOCK DIAGRAM



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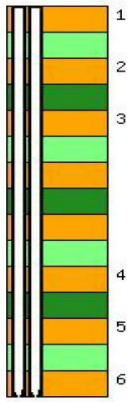
PCB STACKUP

Lay #	Thick (in)	Picture	Type Dk Df	Description	Drill Picture
	0.0006/0.0013		4.5 0.019	Soldermask	
1	0.0020		F / S	0.5oz w/plating	
	0.0032	1080	3.37 0.0096	fill	
2	0.0013		P	1oz	
	0.0030	1080	3.40 0.0095	core	
3	0.0006		S	0.5oz	
	0.0112	2313*2/1080	3.52 0.0092	fill	
	0.0000			None	
	0.0200	2116*4	3.60 0.0090	core	
	0.0000			None	
	0.0115	2313*2/1080	3.50 0.0093	fill	
4	0.0006		S	0.5oz	
	0.0030	1080	3.40 0.0095	core	
5	0.0013		P	1oz	
	0.0031	1080	3.38 0.0096	fill	
6	0.0020		F / S	0.5oz w/plating	
	0.0006/0.0013		4.5 0.019	Soldermask	



0.0639	Total thickness (in) Over mask on plated copper
0.0599	After lamination thickness (in)
0.0613	Over laminate thickness (in) (with soldermask)
0.0650	Customer Requirement (in)
+/-0.0063	Customer Tolerance (in)

Impedance Constraint Information (I)

Imp #	Impedance Type		Affect Lyr (1)	Affect Lyr (2)	Cust L/W	Line Width (1)	Line Width (2)	CenterToCenter (1)	CenterToCenter (2)	Ref Plane Top	Ref Plane Bot	Targ ohms	Tol ohms	Predicted ohms@2GHz
1	EC MS		1	None	0.004	0.004	0.004	0.0088		None	2	90	9	90.59
2	EC MS		1	None	0.004	0.004	0.004	0.012		None	2	100	10	100.66
3	Surf MS		1	None	0.005	0.005				None	2	50	5	50.99
4	EC SL		3	None	0.0047	0.0047	0.0047	0.0101		5	2	90	9	89.51
5	EC SL		3	None	0.0044	0.0044	0.0044	0.0124		5	2	97	9.7	97.11
6	EC SL		3	None	0.0044	0.0044	0.0044	0.0146		5	2	100	10	99.43
7	Stripline		3	None	0.005	0.005				5	2	50	5	49.53
8	EC SL		4	None	0.0047	0.0047	0.0047	0.0101		2	5	90	9	89.51
9	EC SL		4	None	0.0044	0.0044	0.0044	0.0124		2	5	97	9.7	97.11
10	EC SL		4	None	0.0044	0.0044	0.0044	0.0146		2	5	100	10	99.43
11	Stripline		4	None	0.005	0.005				2	5	50	5	49.53
12	EC MS		6	None	0.004	0.004	0.004	0.0088		None	5	90	9	89.49
13	EC MS		6	None	0.004	0.004	0.004	0.012		None	5	100	10	99.16
14	Surf MS		6	None	0.005	0.005				None	5	50	5	49.97

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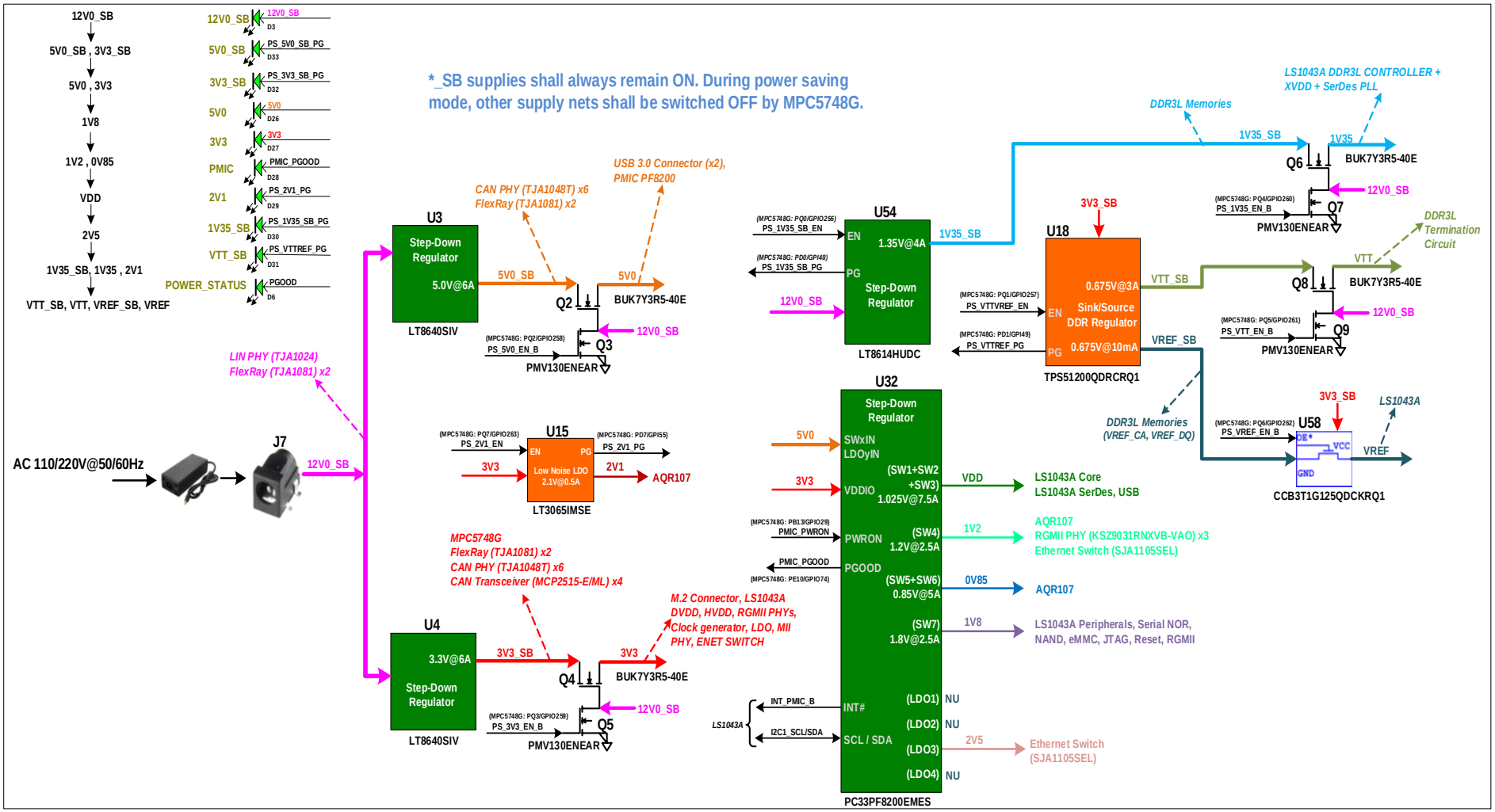
POWER SUPPLY ARCHITECTURE



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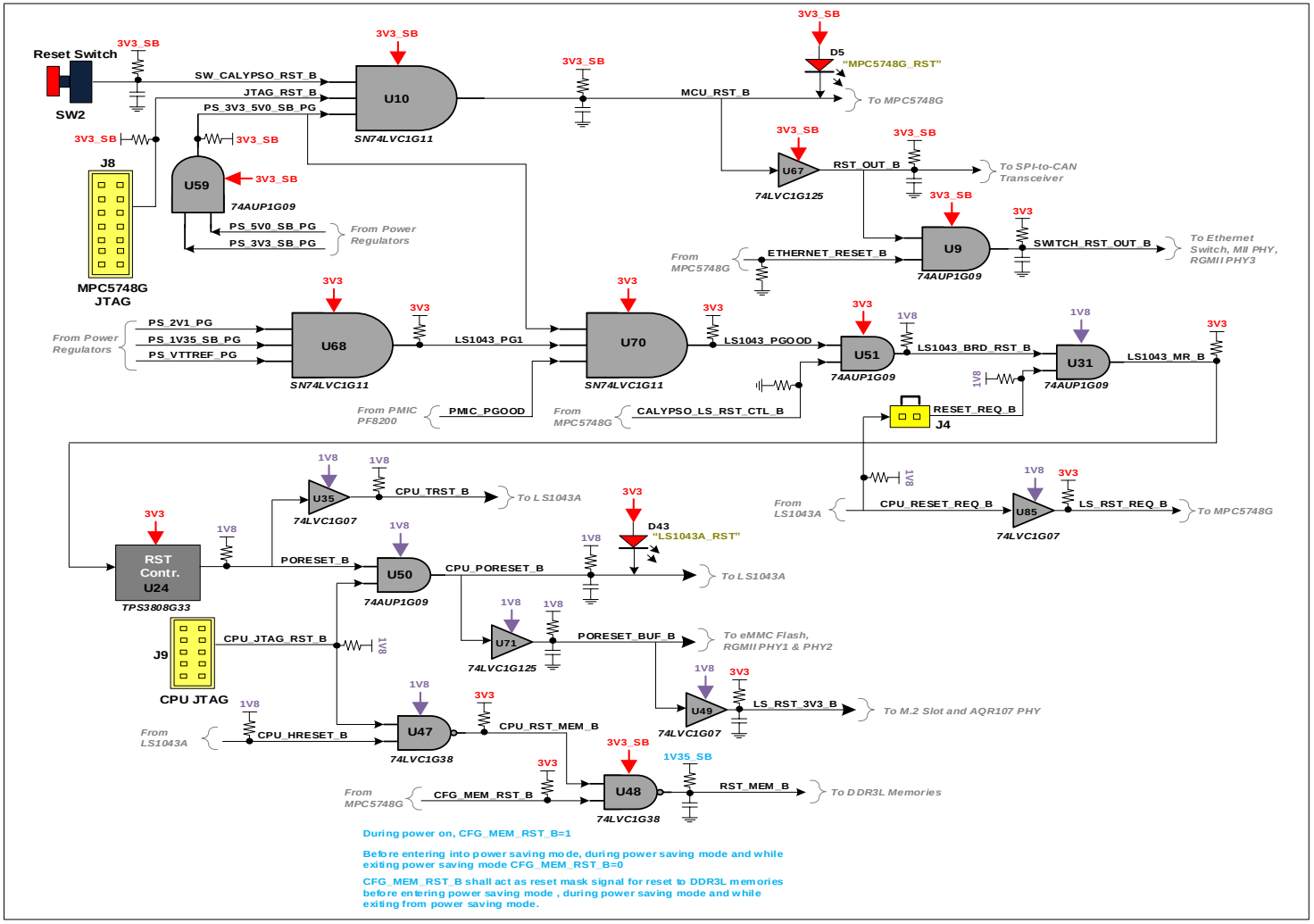
RESET ARCHITECTURE



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Page Title: **RESET ARCHITECTURE**

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AC ADAPTER SPECIFICATIONS

DC Voltage Output: 12VDC

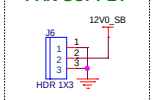
Current Output: ~ 5A (depending on application)

Polarity:

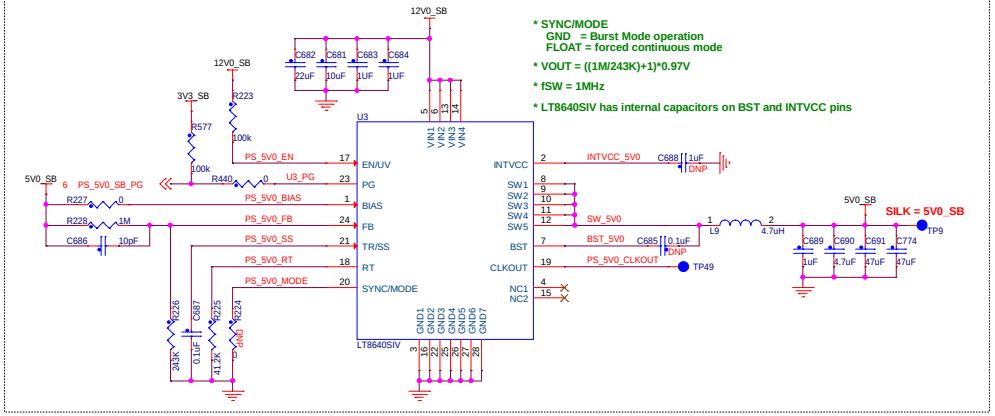
Inner Diameter: 2.1mm

Outer Diameter: 5.5mm

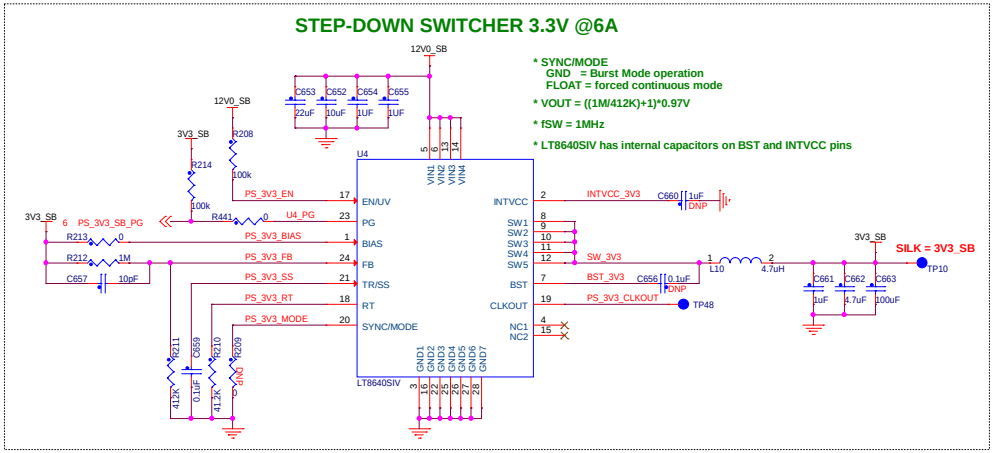
FAN SUPPLY



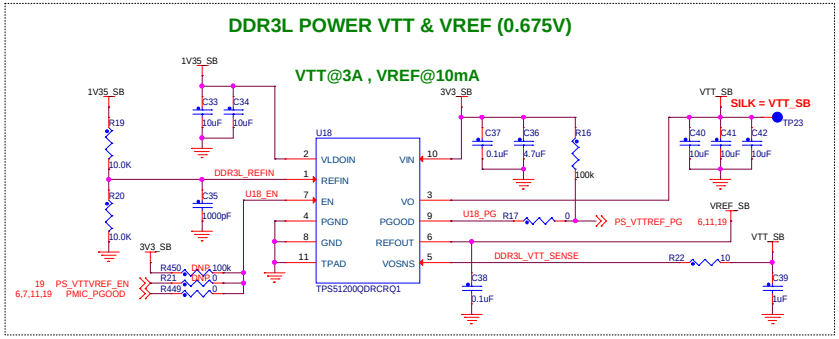
STEP-DOWN SWITCHER 5V @6A



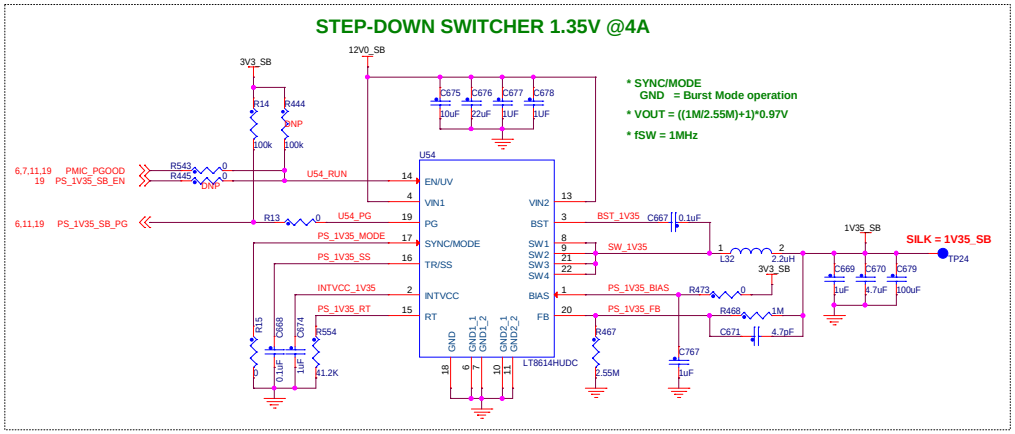
STEP-DOWN SWITCHER 3.3V @6A

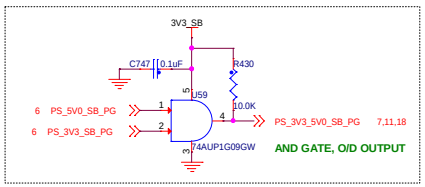


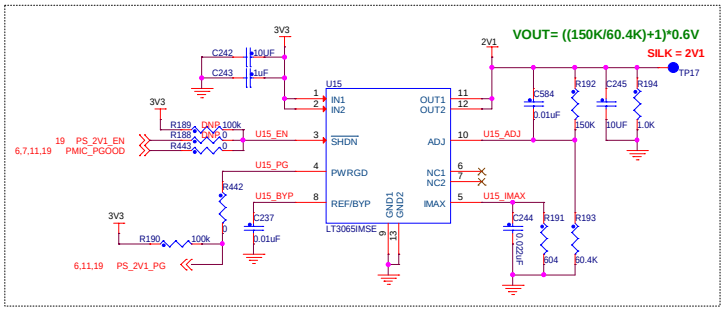
DDR3L POWER VTT & VREF (0.675V)

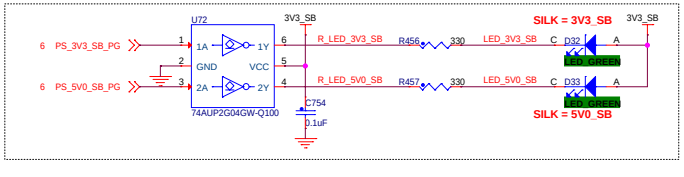


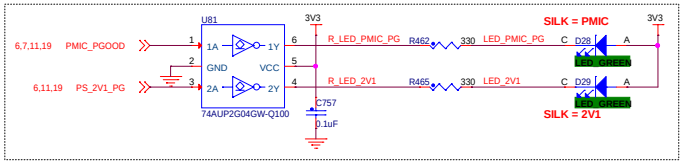
STEP-DOWN SWITCHER 1.35V @4A

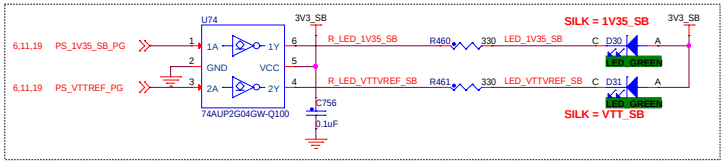


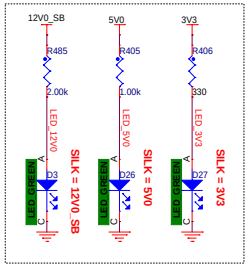












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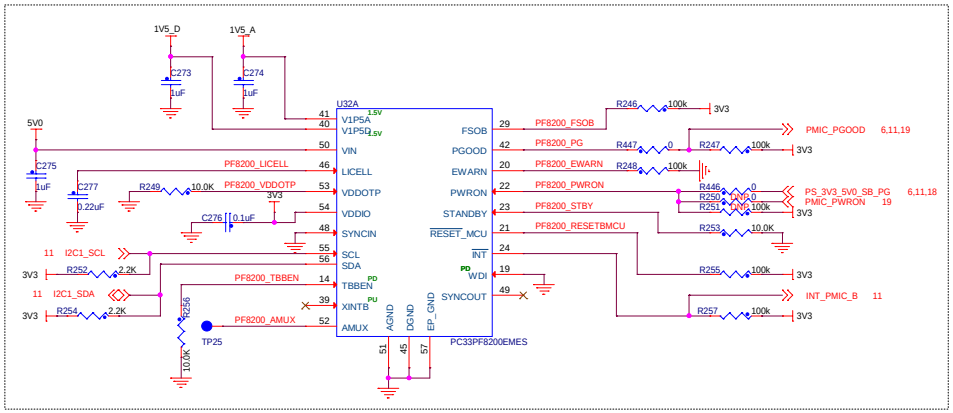
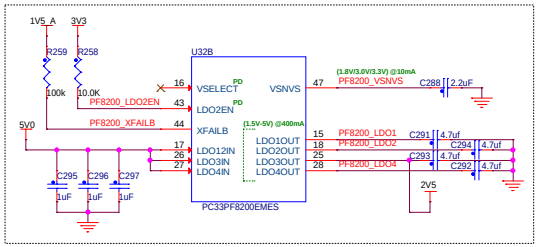
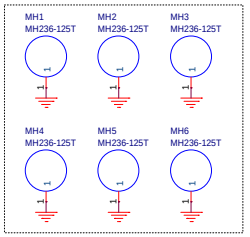
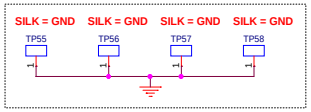
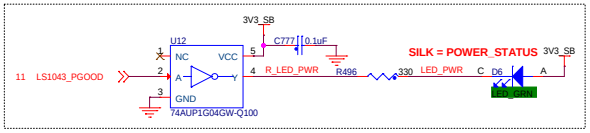
PMIC & POWER GATING

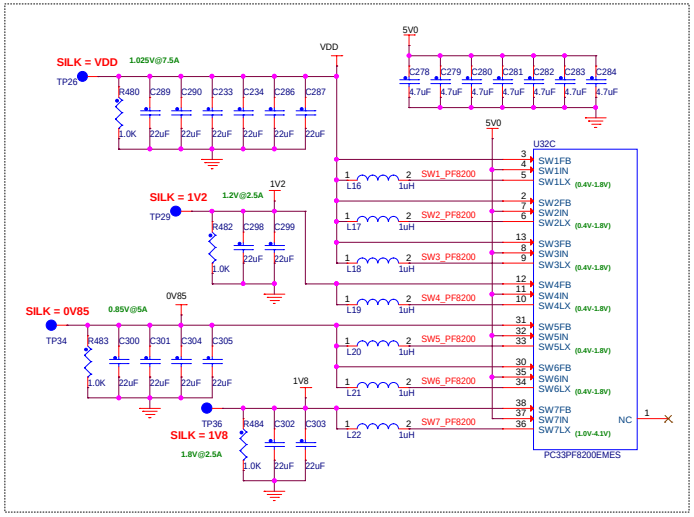


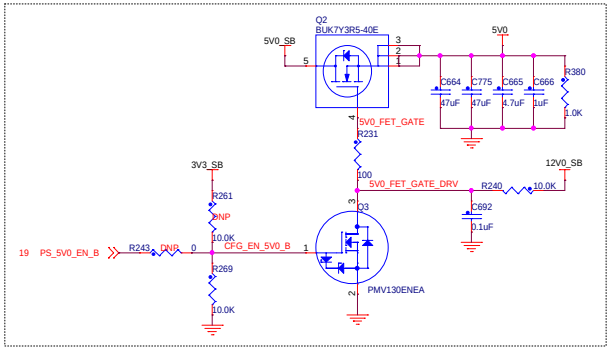


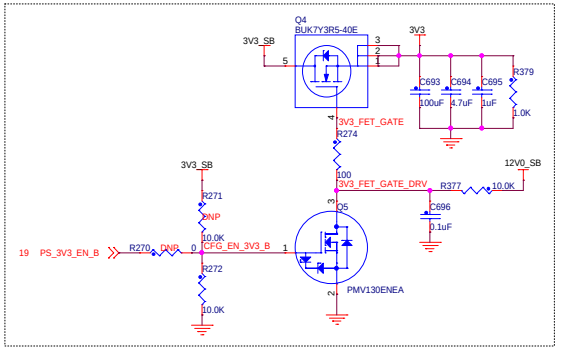


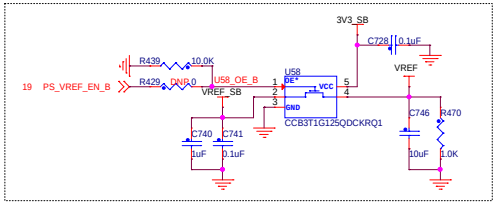


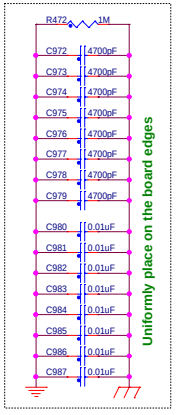


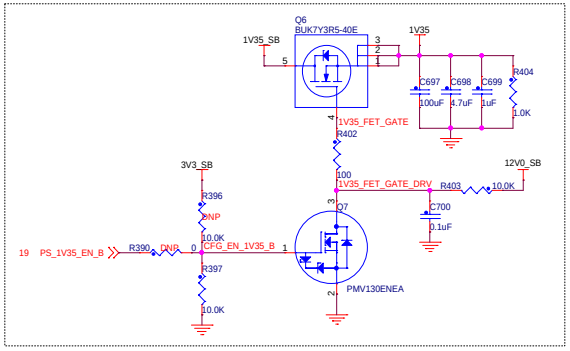


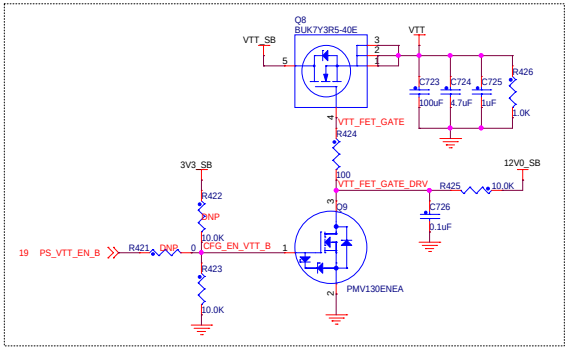












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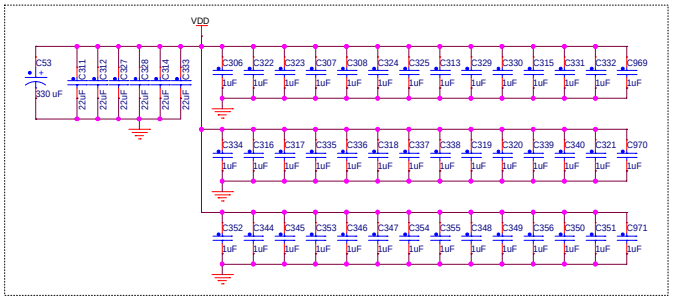
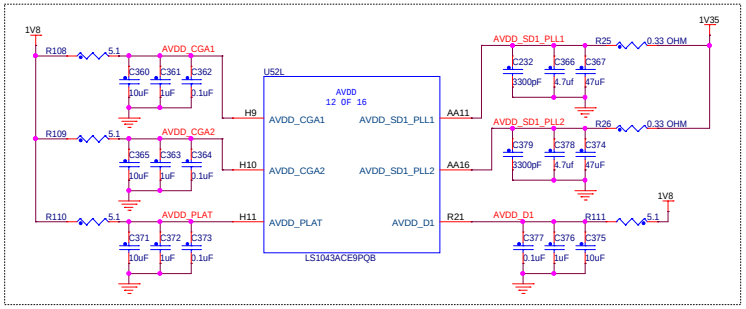
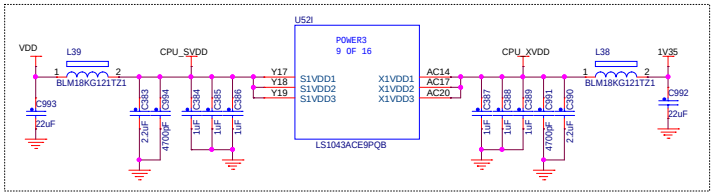
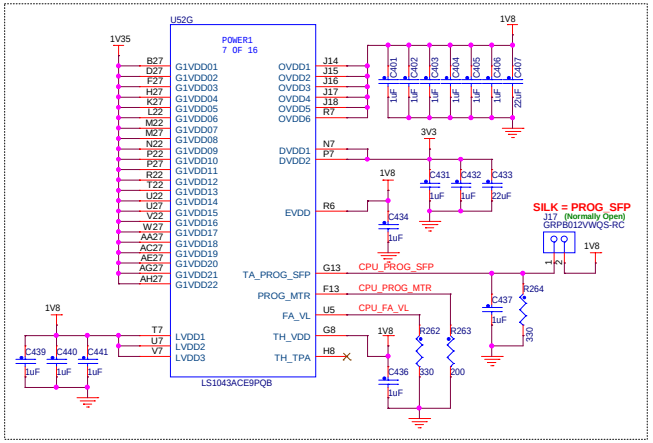
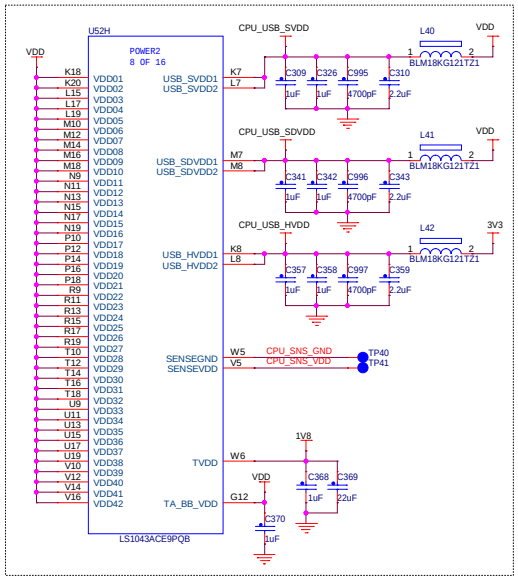
LS1043A POWER

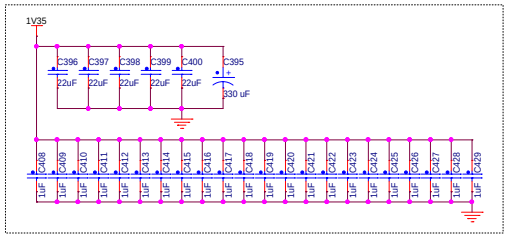


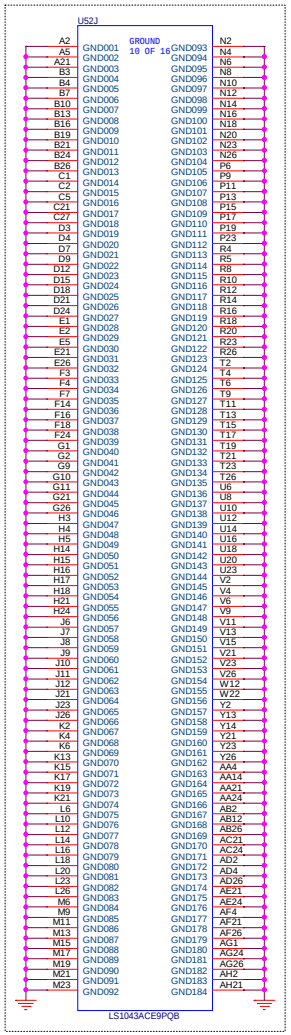


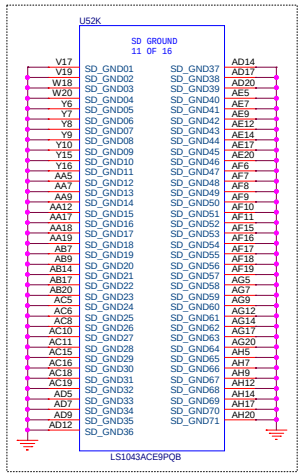


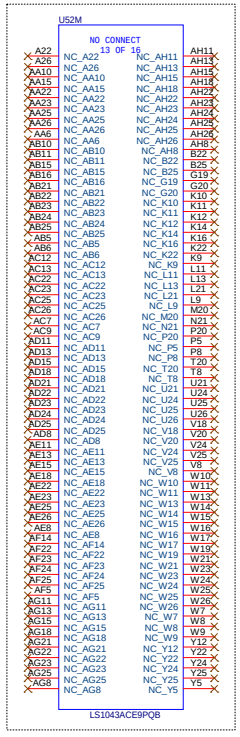












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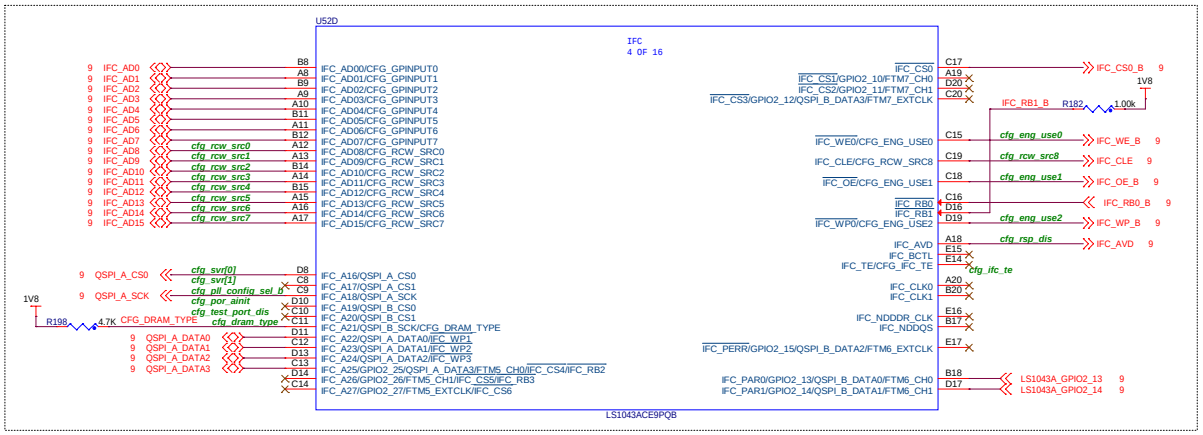
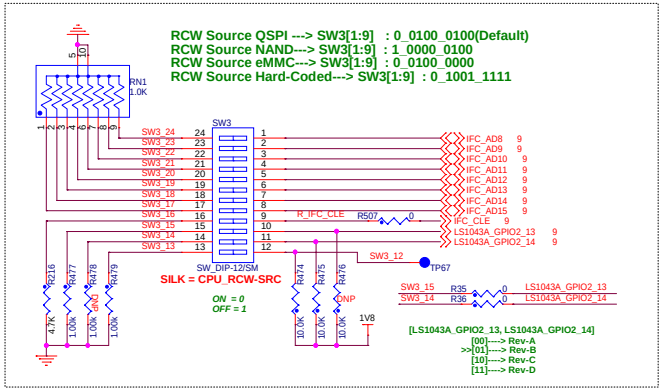
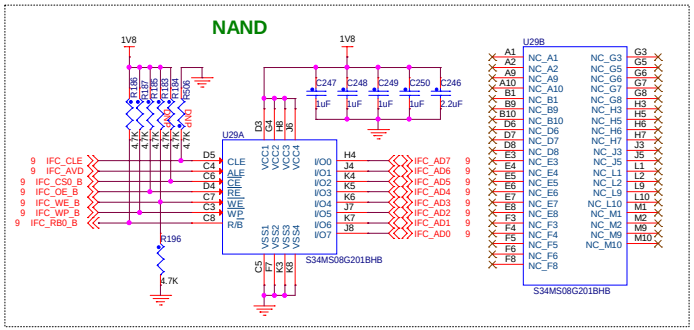
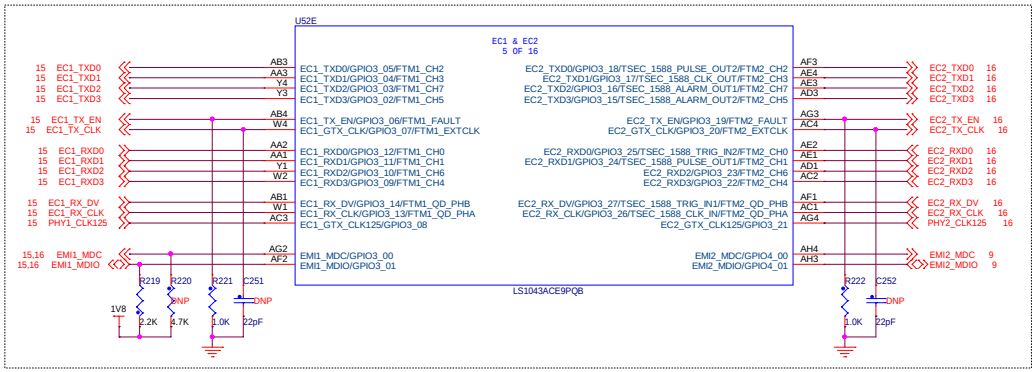
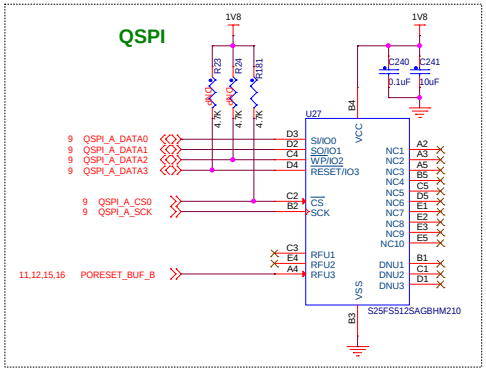
LS1043A IFC, QSPI, RGMII, SERDES

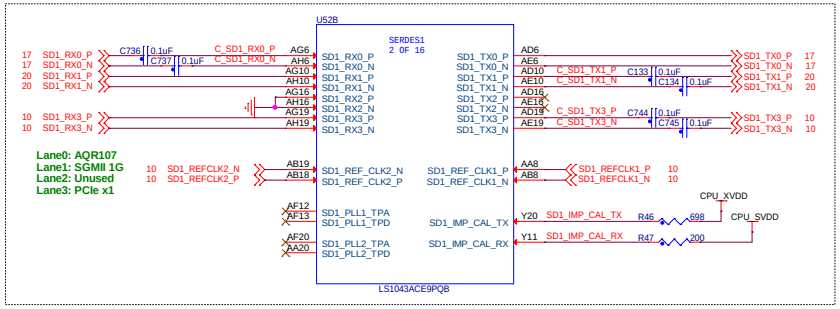


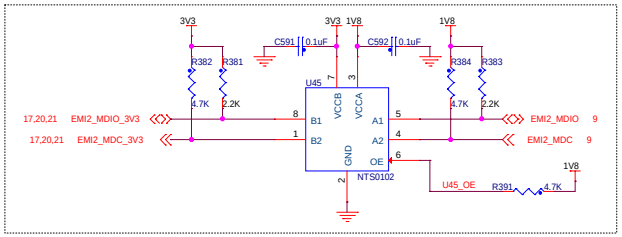












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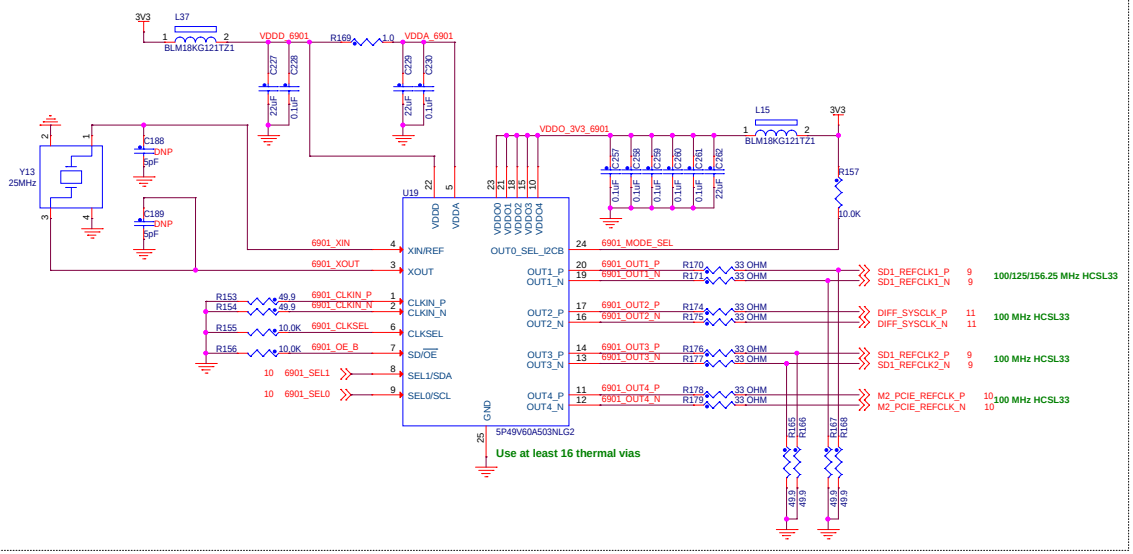
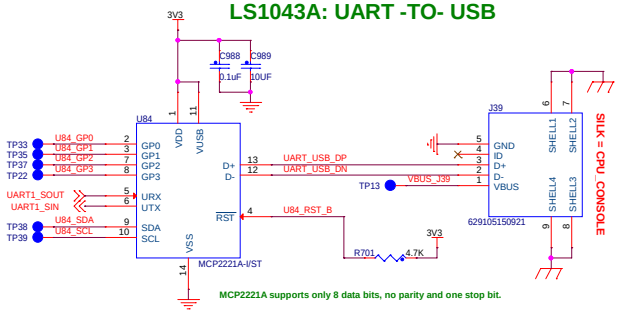
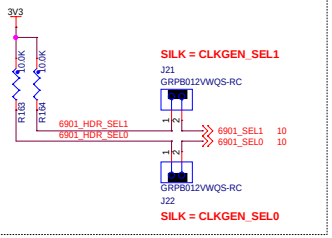
DIFF_SYSCLK & SERDES REFCLK GENERATION



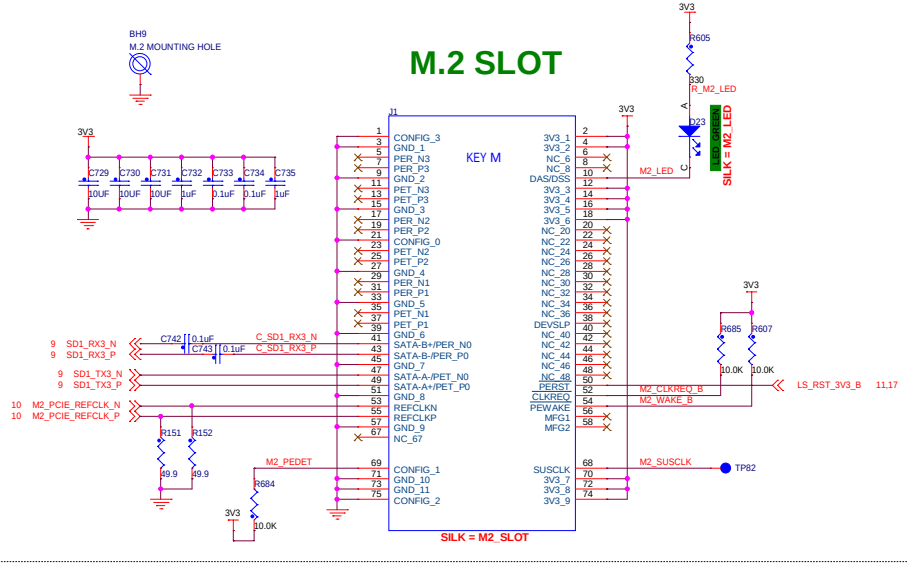
LS1043A: UART -TO- USB

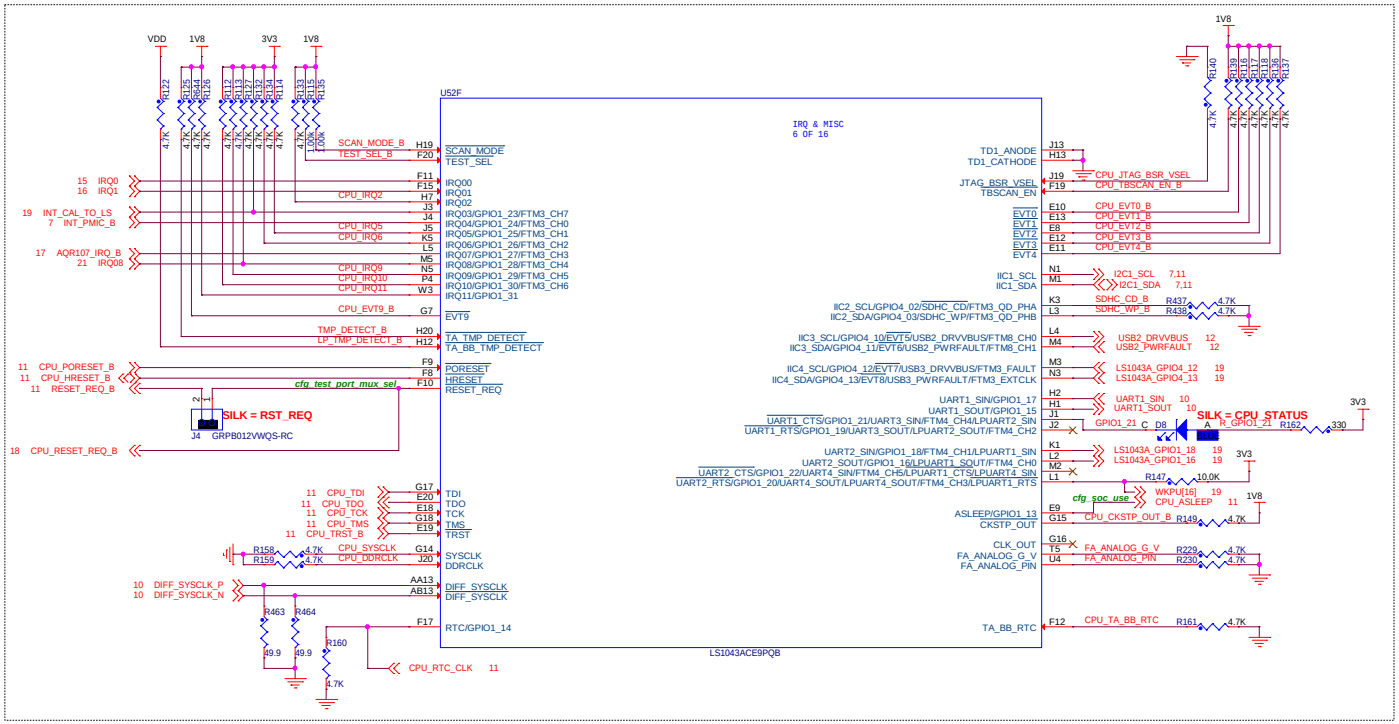


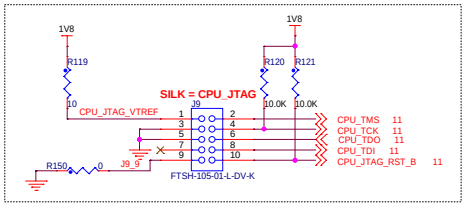


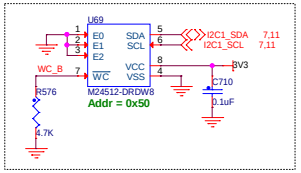
J21	J22	SD1_REFCLK1
OPEN	OPEN	156.25 MHz
OPEN	SHORT	125 MHz
SHORT	OPEN	100 MHz
SHORT	SHORT	156.25 MHz

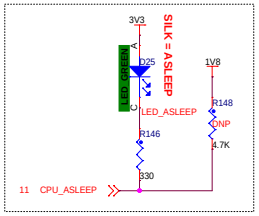
M.2 SLOT

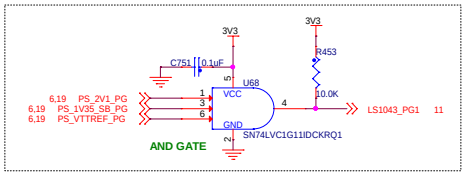


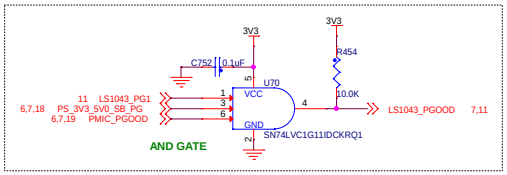


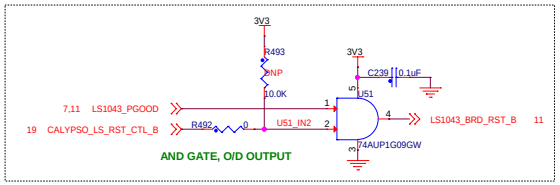


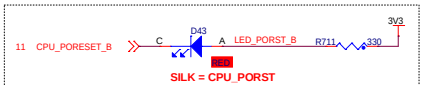


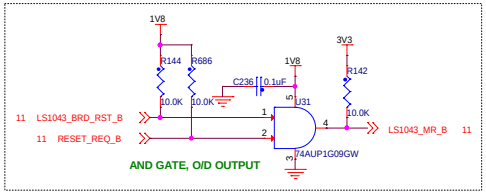


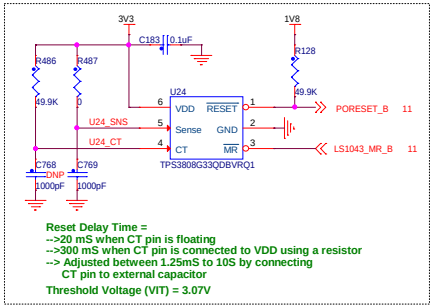


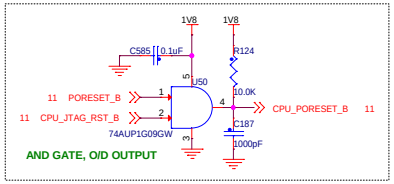


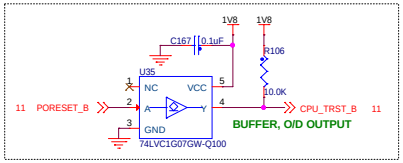


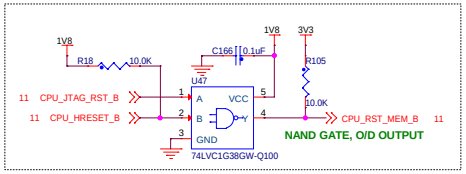


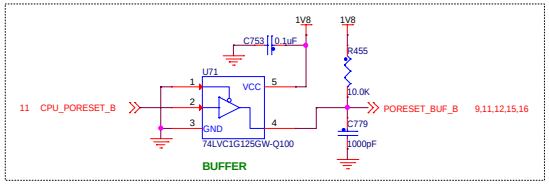


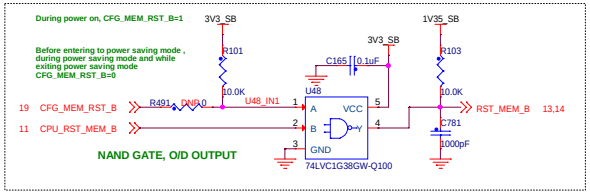


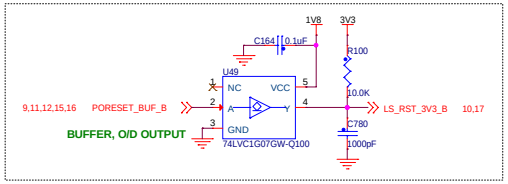


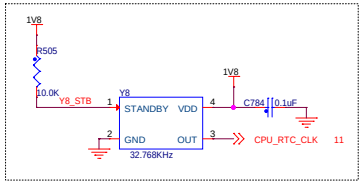












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Page Title:	LS1043A MISC_RESET		
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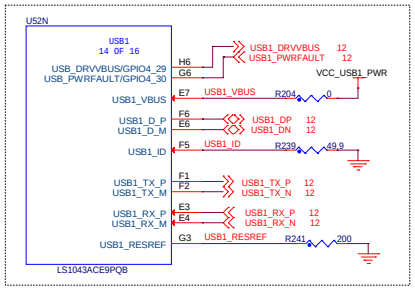
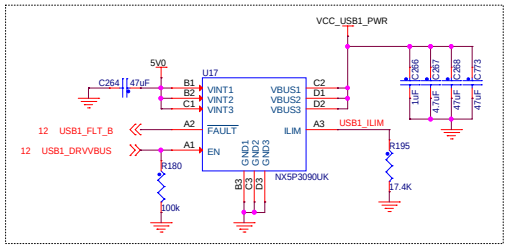
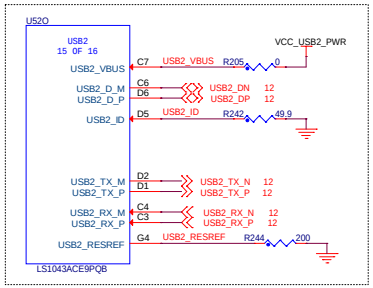
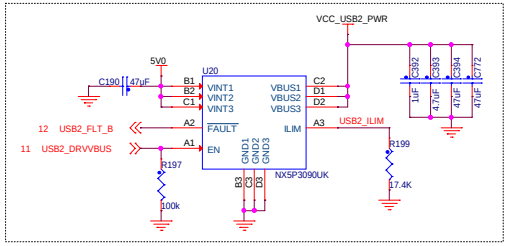
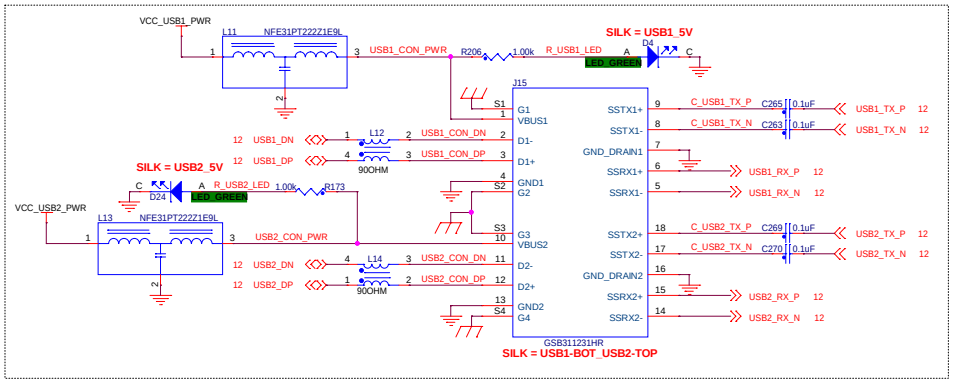
LS1043A USB 3.0 & eMMC

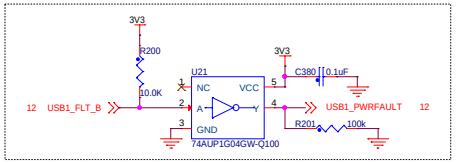


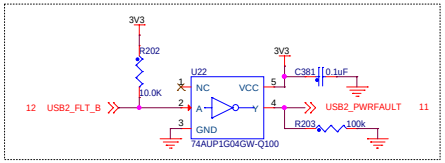


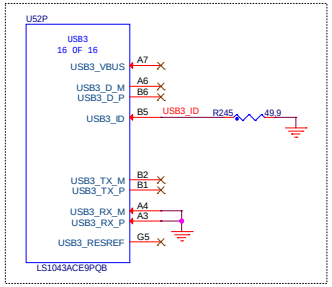


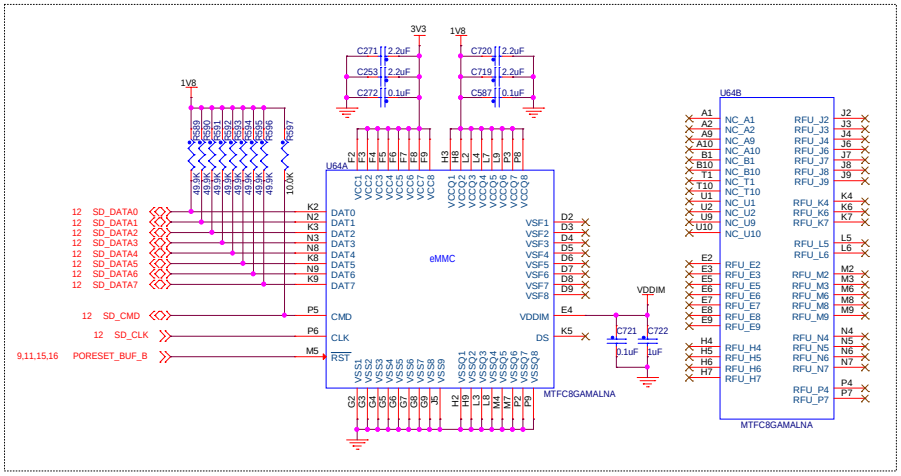


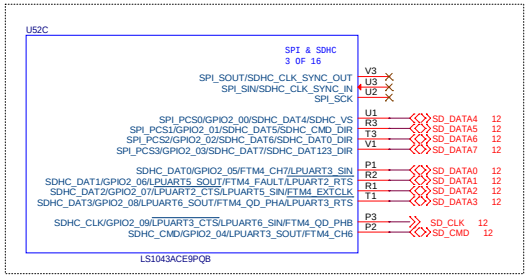


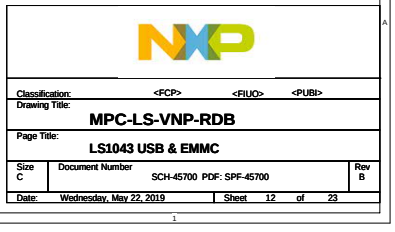




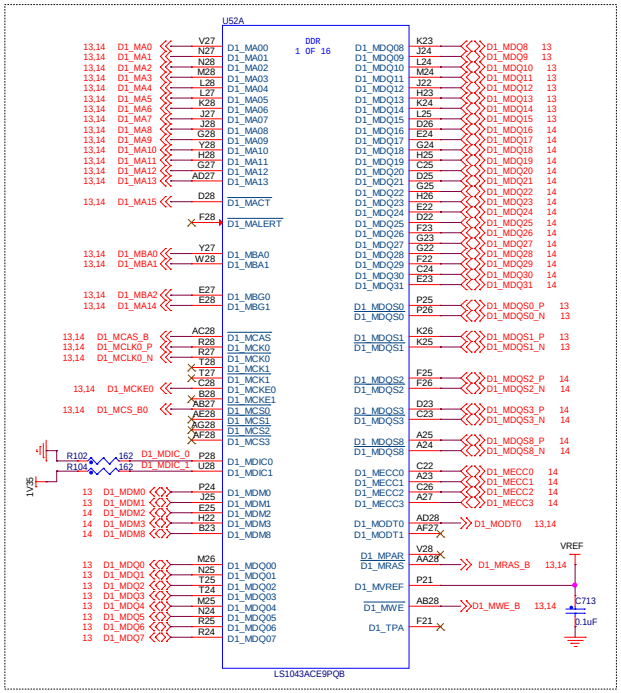


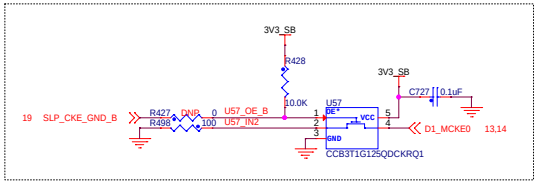


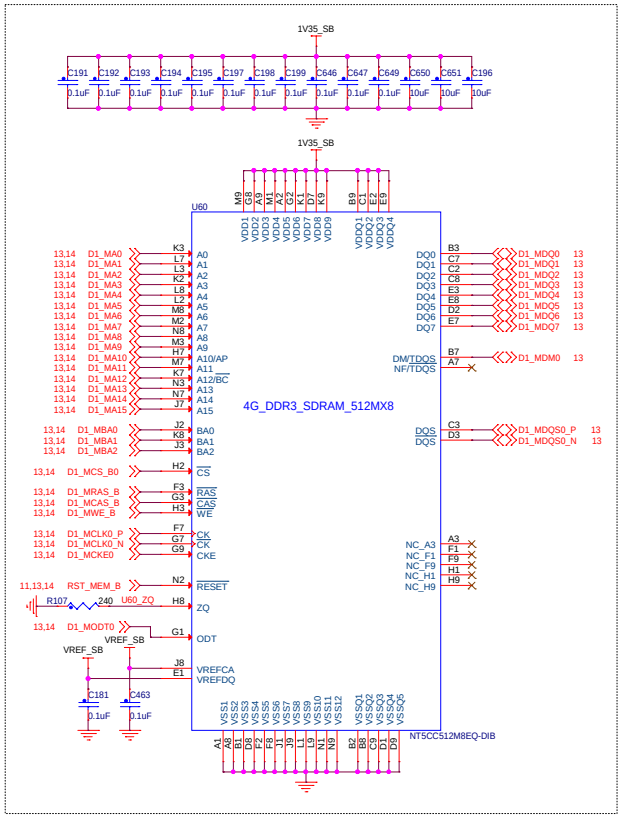


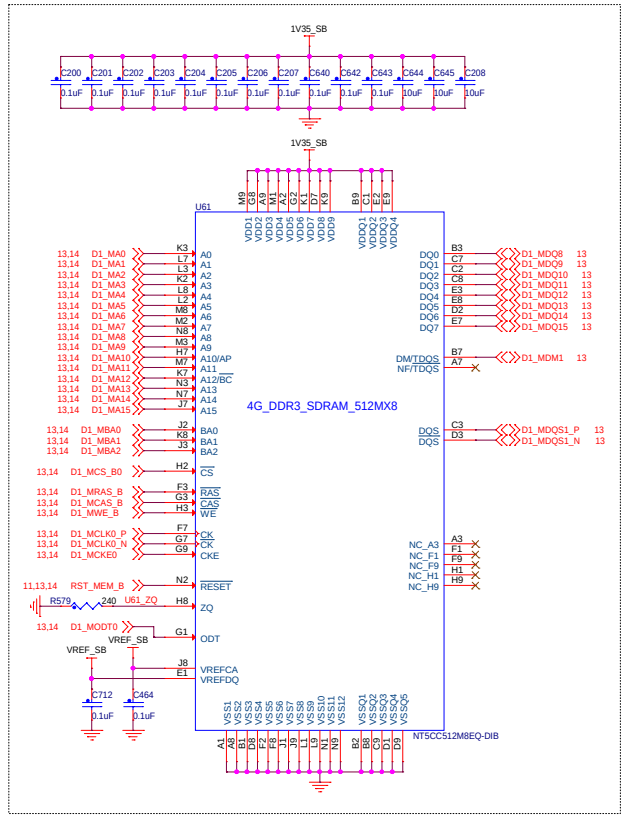


LS1043A DDR3L & MEMORY









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Page Title:	LS1043A DDR3L & MEMORIES#1		
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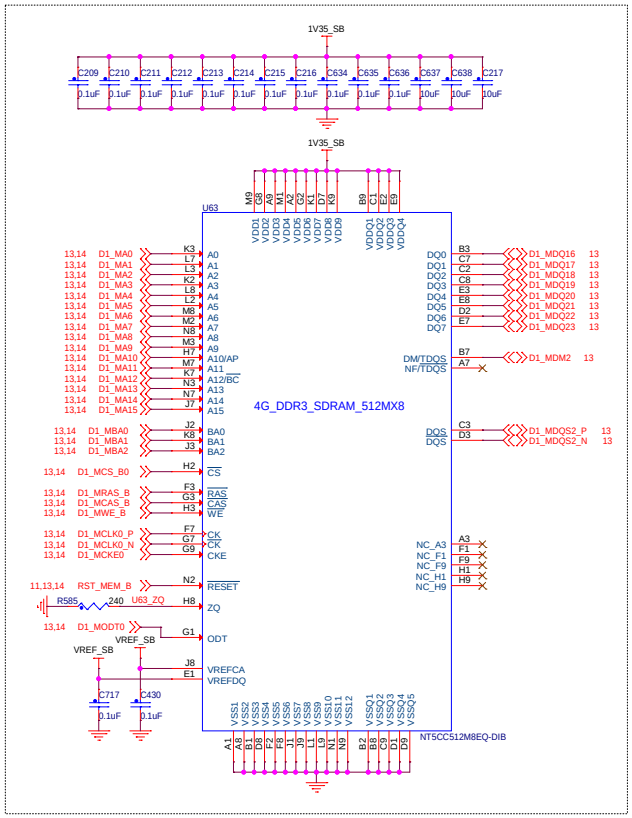
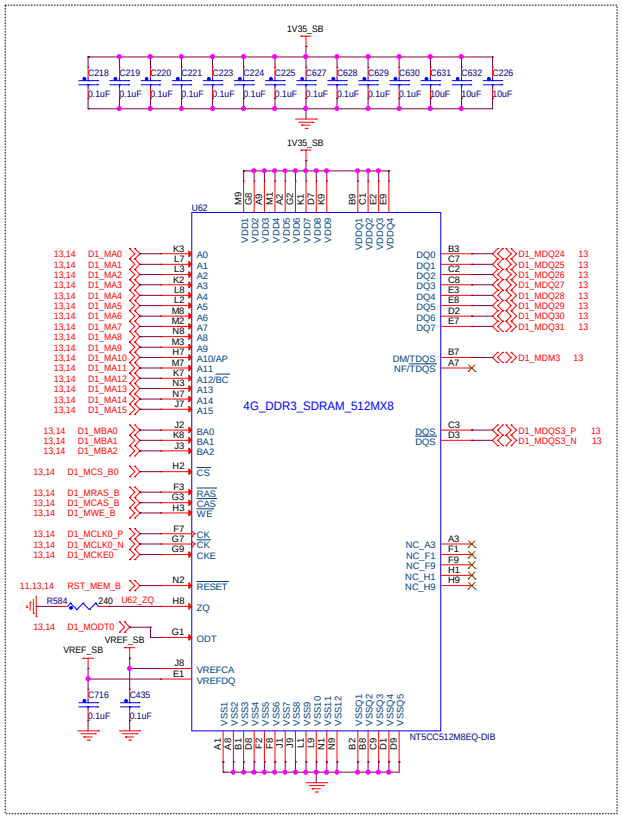
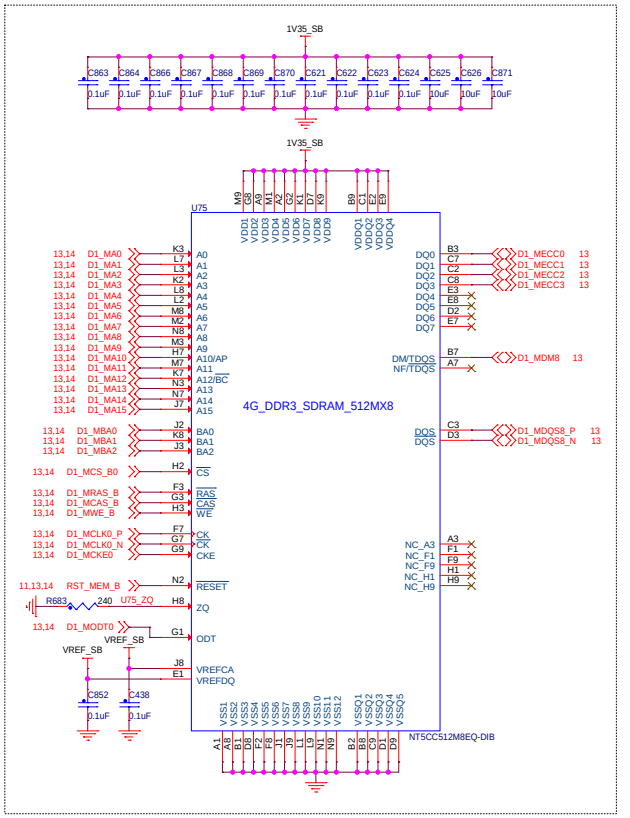
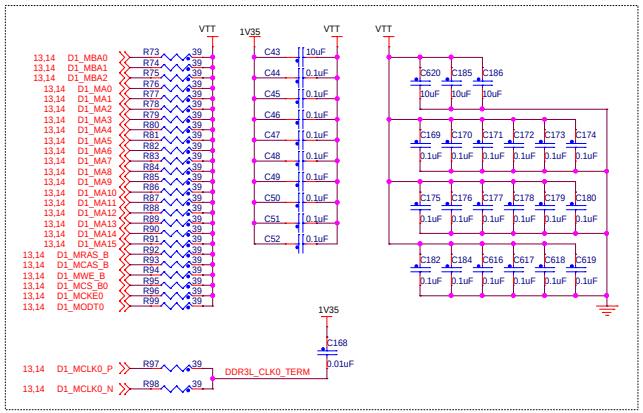
DDR3L MEMORY









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Page Title:	DDR3L MEMORIES#2		
Size: C	Document Number: SCH-45700 PDF: SPF-45700		Rev: B
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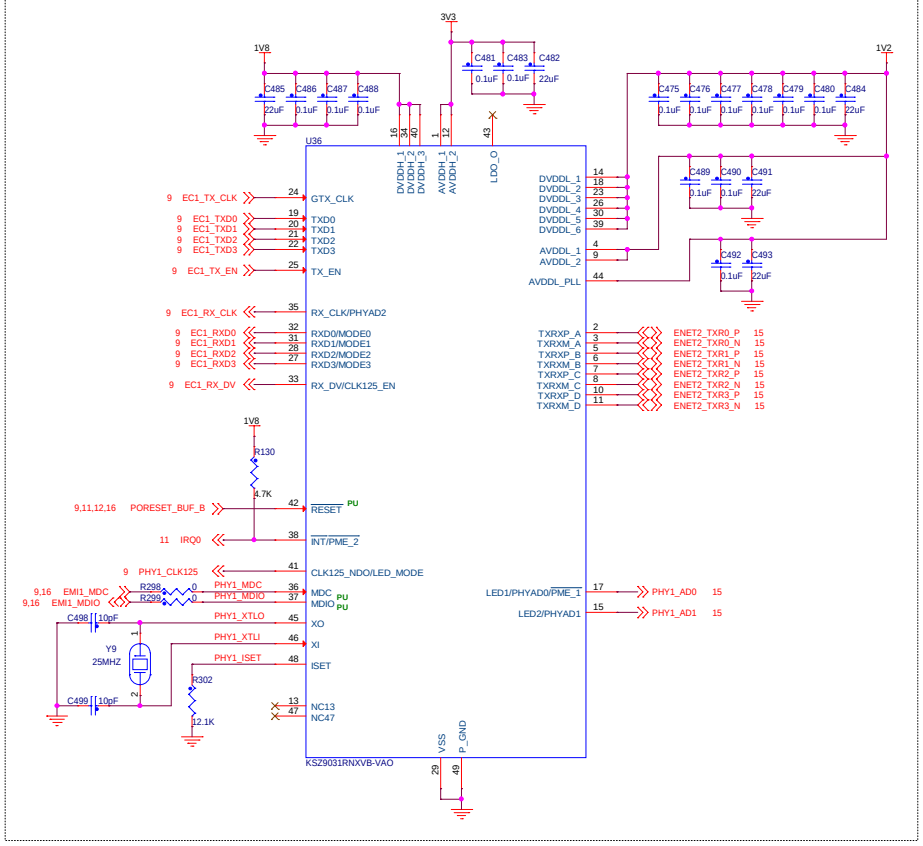
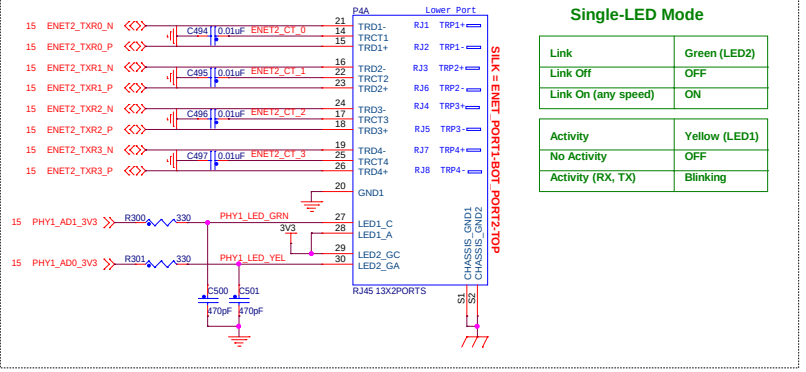
LS1043A - RGMII PHY#1

The recommended power-up sequence is to have the transceiver (AVDDH) and digital I/O (DVDDH) voltages power up before the 1.2V core (DVDDL, AVDDL, AVDDL_PLL) voltage.

There is no power sequence requirement between transceiver (AVDDH) and digital I/O (DVDDH) power rails.



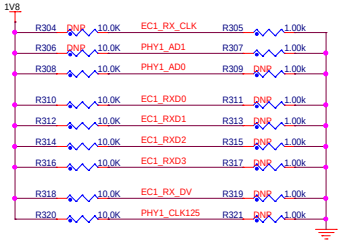


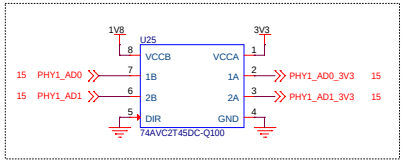
Single-LED Mode

Link	Green (LED2)
Link Off	OFF
Link On (any speed)	ON

Activity	Yellow (LED1)
No Activity	OFF
Activity (RX, TX)	Blinking

PIN	DESCRIPTION	DEFAULT CONFIGURATION
RX_CLK (PHYAD2) LED2 (PHYAD1) LED1 (PHYAD0)	PHY ADDRESS [2:0]:State of PHYADx Pins are latched into PHYCTRL register at system Hardware-Reset. Note PHY Address Bits [4:3] are always set to '00'	001
RXD3 (MODE3) RXD2 (MODE2) RXD1 (MODE1) RXD0 (MODE0)	0100 NAND tree 0111 Chip power-down 1100 RGMII,1000BT FD only 1101 RGMII,1000BT FD/HD only 1110 RGMII,all except 1000BT HD 1111 RGMII,all (10/100/1000 speed HD/FD) Others Reserved	1111
RX_DV (CLK125_EN)	1 = Enable 125 MHz clock output 0 = Disable 125 MHz clock output	1
CLK125_NDO (LED_MODE)	1 = Single-LED mode 0 = Tri-color dual-LED mode	1





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Page Title:	LS1043A_EC1_RGMII_PHY		
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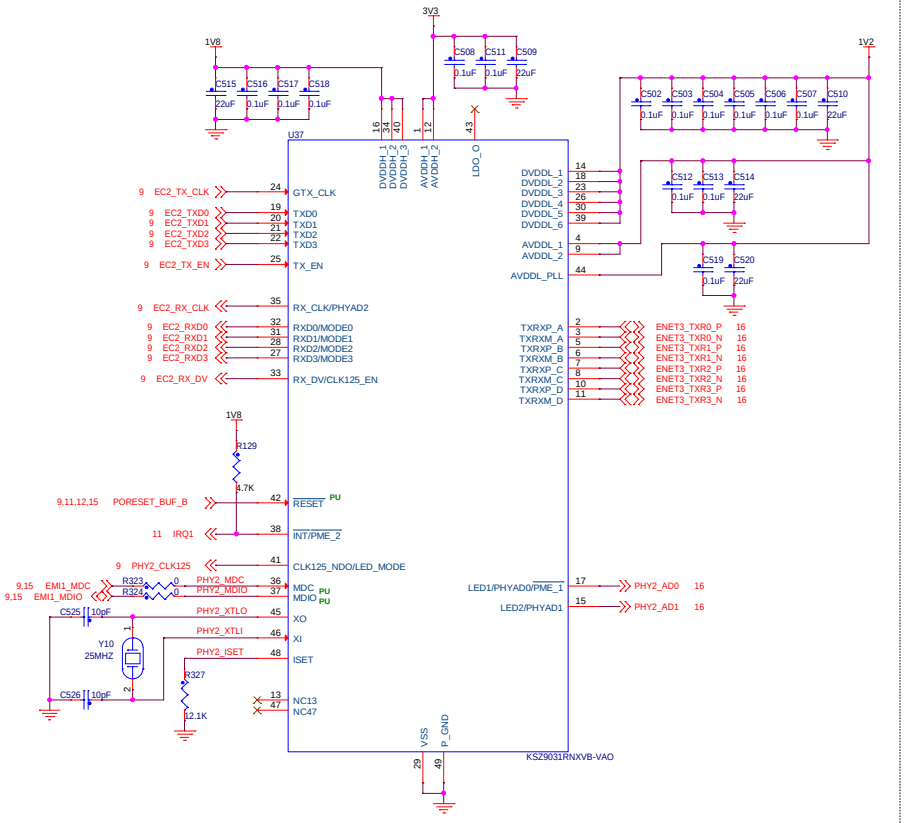
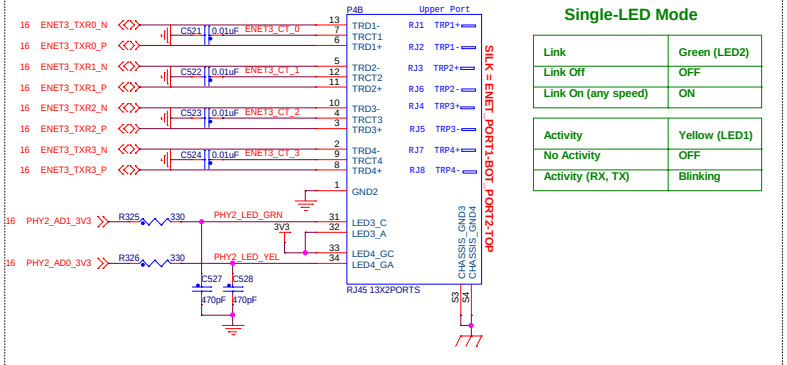
LS1043A - RGMII PHY#2

The recommended power-up sequence is to have the transceiver (AVDDH) and digital I/O (DVDDH) voltages power up before the 1.2V core (DVDDL, AVDDL, AVDDL_PLL) voltage.

There is no power sequence requirement between transceiver (AVDDH) and digital I/O (DVDDH) power rails.



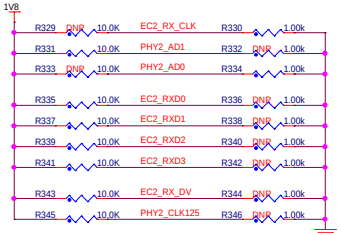


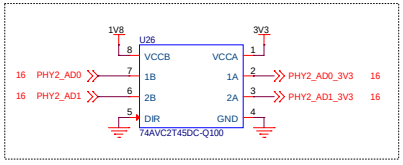
Single-LED Mode

Link	Green (LED2)
Link Off	OFF
Link On (any speed)	ON

Activity	Yellow (LED1)
No Activity	OFF
Activity (RX, TX)	Blinking

PIN	DESCRIPTION	DEFAULT CONFIGURATION
RX_CLK (PHYAD2) LED2 (PHYAD1) LED1 (PHYAD0)	PHY ADDRESS [2:0]:State of PHYADx Pins are latched into PHYCTRL register at system Hardware-Reset. Note PHY Address Bits [4:3] are always set to '00'	010
RXD3 (MODE3) RXD2 (MODE2) RXD1 (MODE1) RXD0 (MODE0)	0100 NAND tree 0111 Chip power-down 1100 RGMII,1000BT FD only 1101 RGMII,1000BT FD/HD only 1110 RGMII,all except 1000BT HD 1111 RGMII,all (10/100/1000 speed HD/FD) Others Reserved	1111
RX_DV (CLK125_EN)	1 = Enable 125 MHz clock output 0 = Disable 125 MHz clock output	1
CLK125_NDO (LED_MODE)	1 = Single-LED mode 0 = Tri-color dual-LED mode	1





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Page Title:	LS1043A_EC2_RGMII_PHY		
Size: C	Document Number: SCH-45700 PDF: SPF-45700		Rev: B
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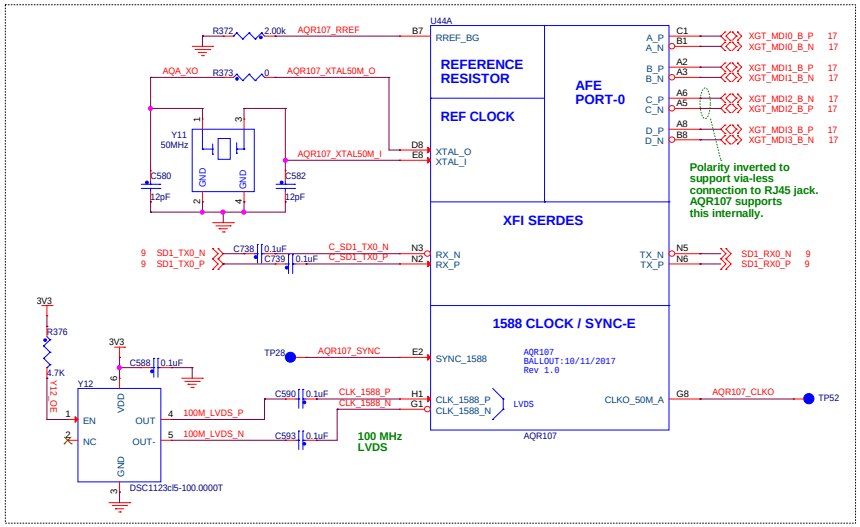
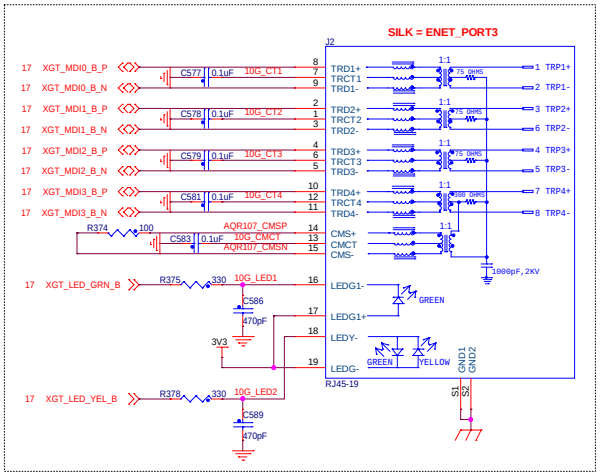
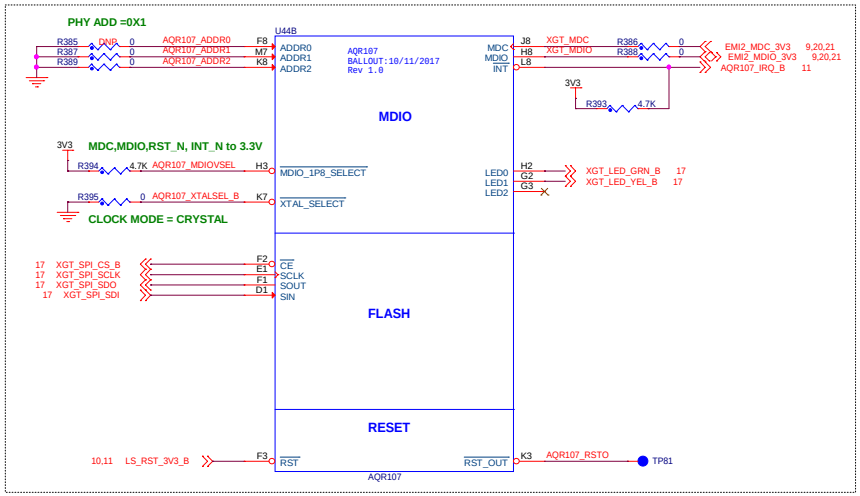
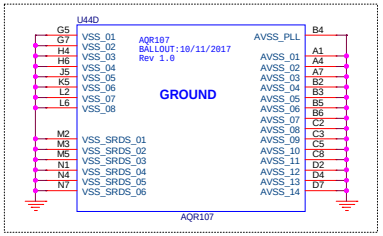
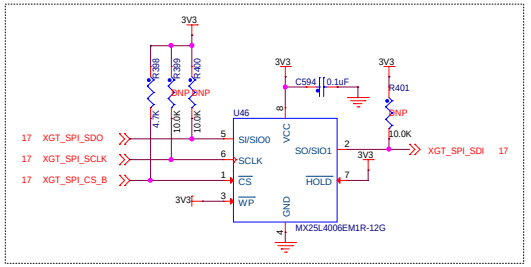
AQR107

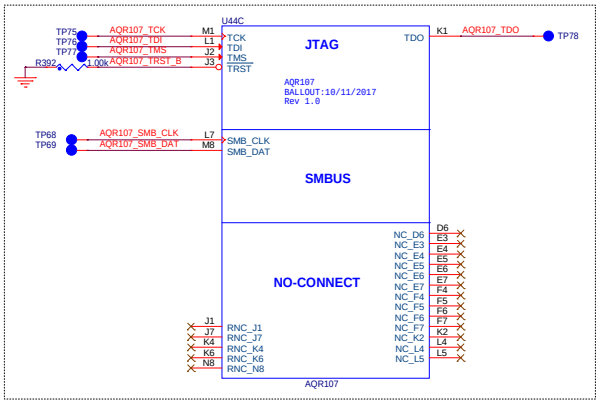


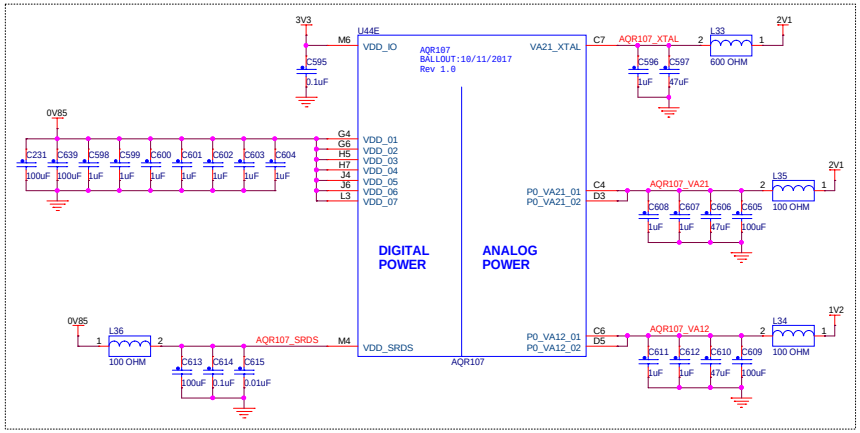












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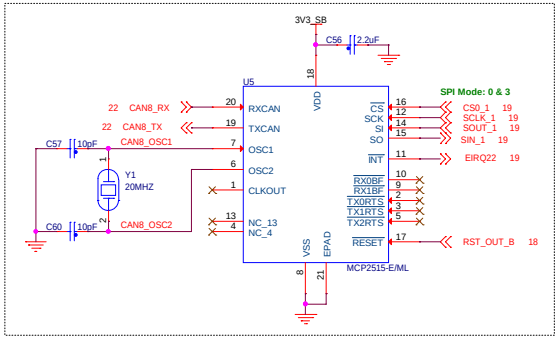
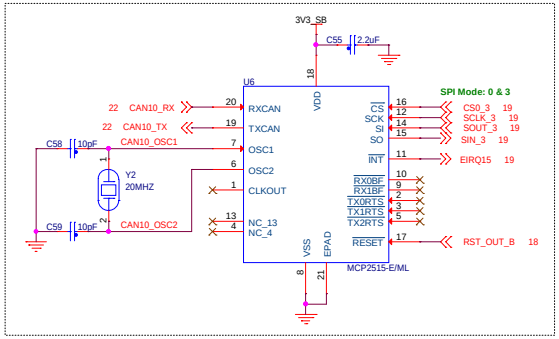
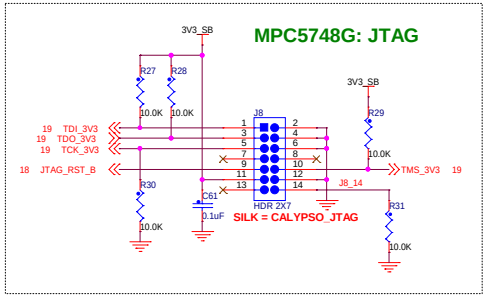
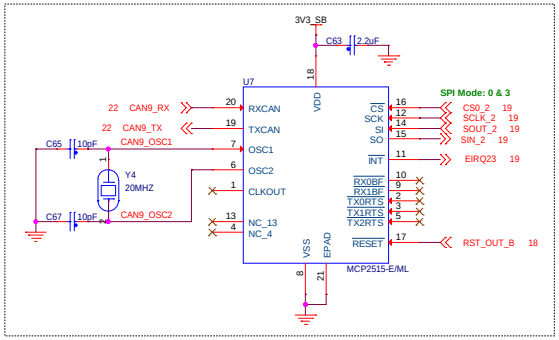
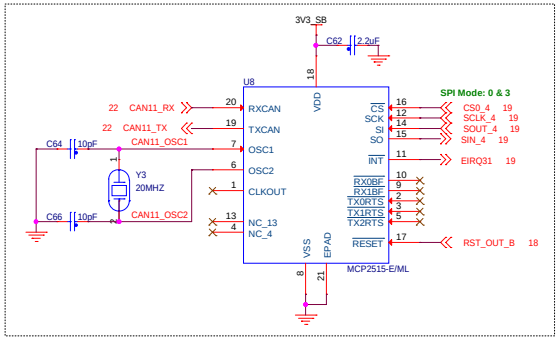
MPC5748G RESET, JTAG, CAN TRANSCEIVER

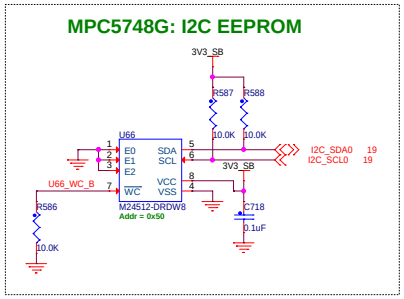


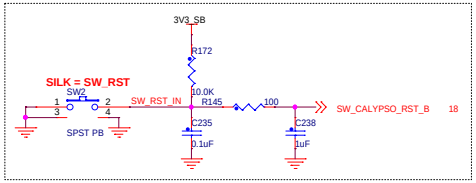


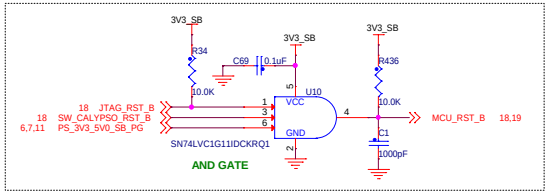


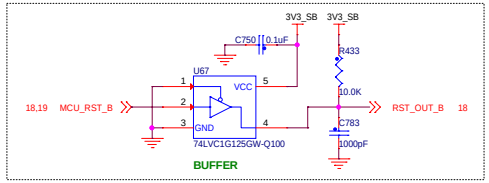


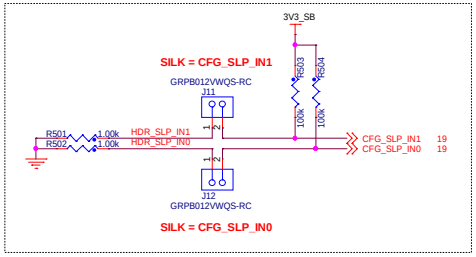


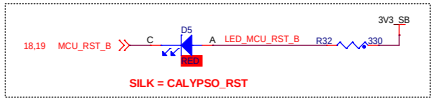


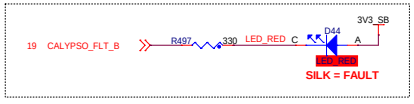


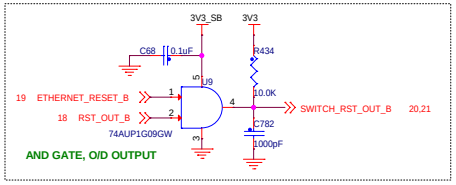


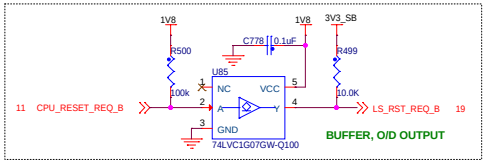












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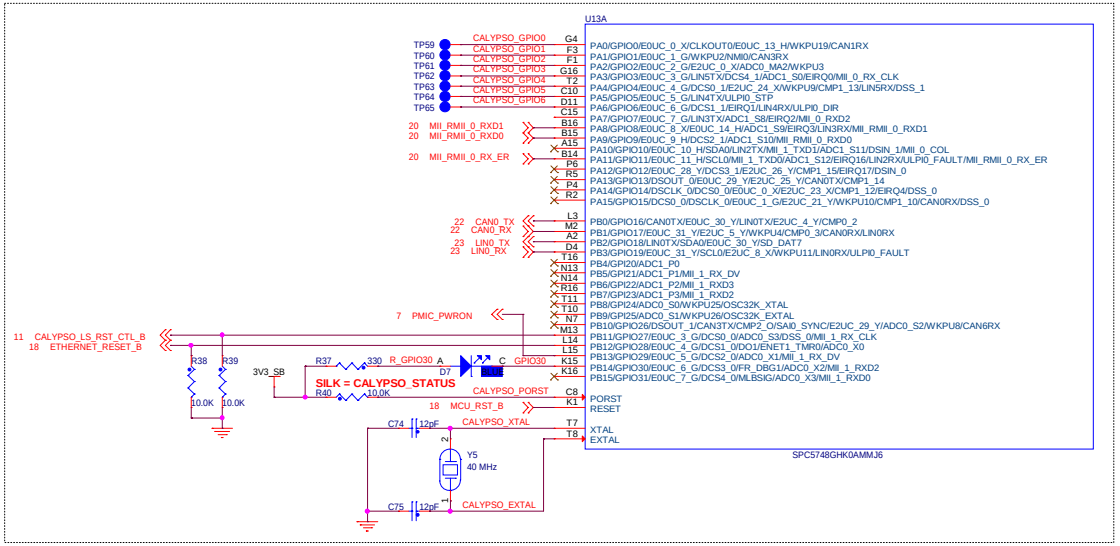

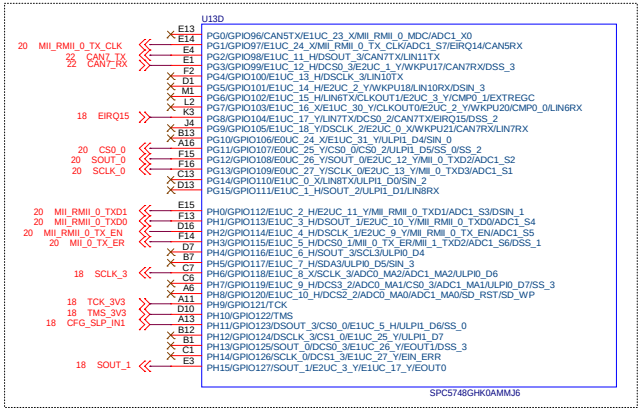

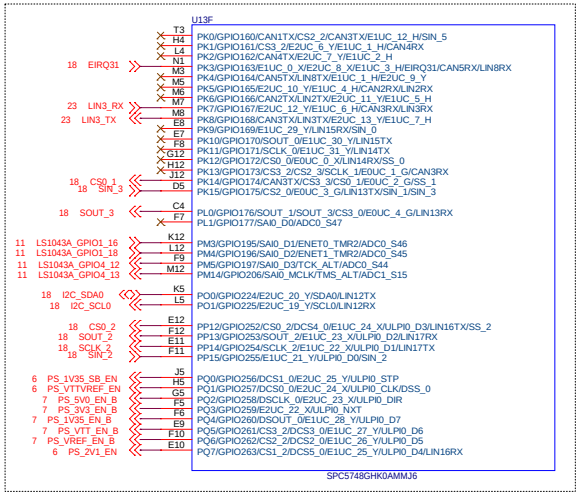

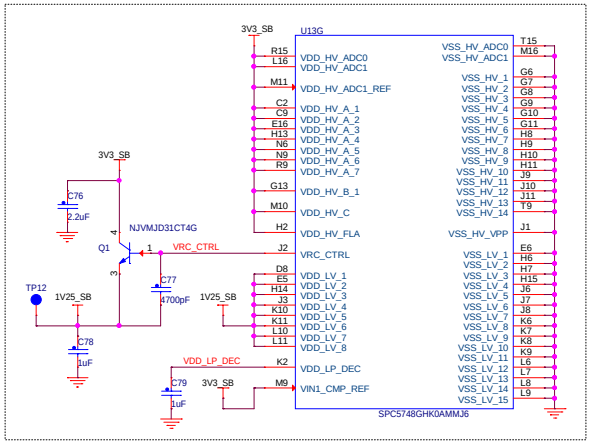

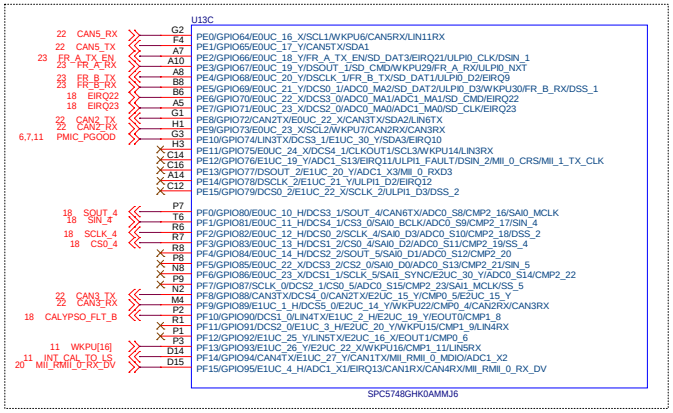

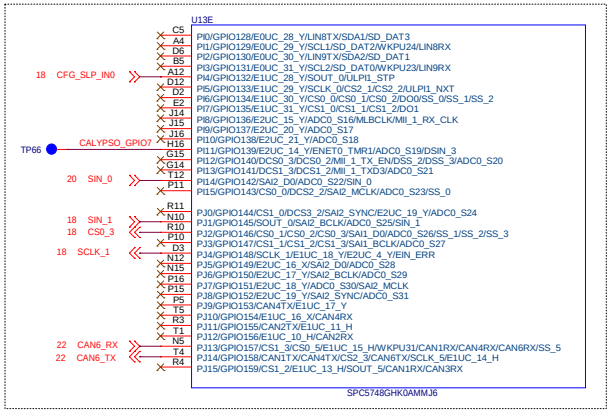

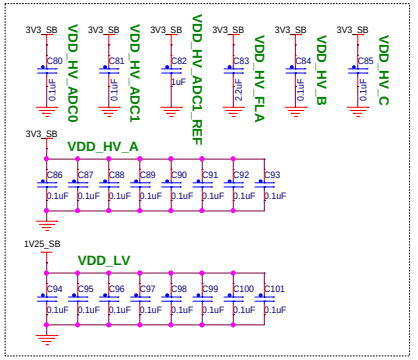

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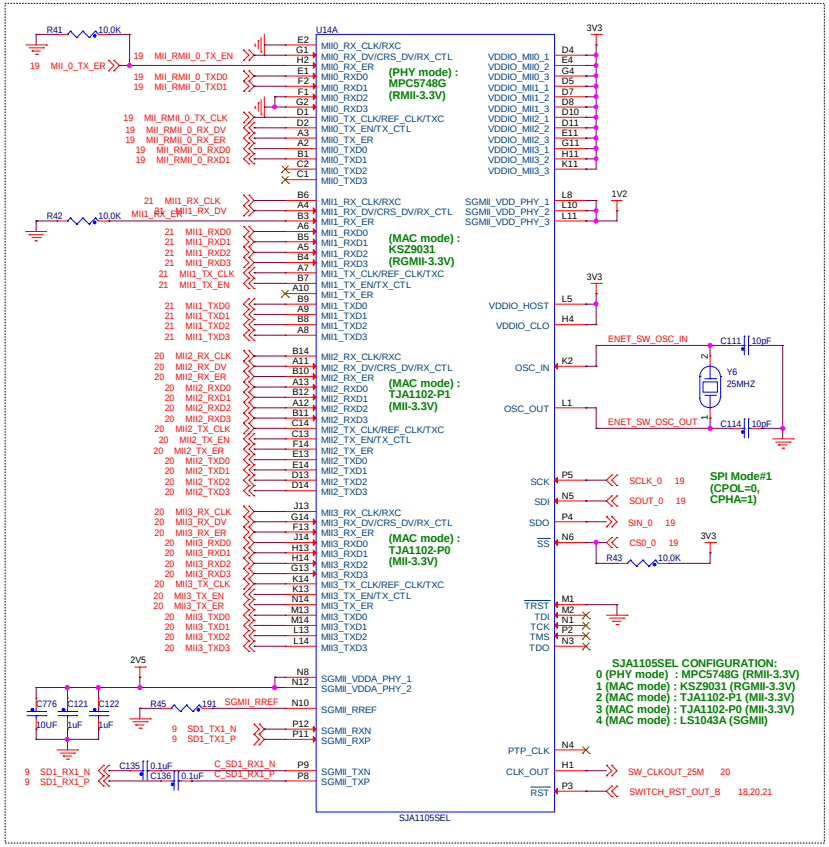
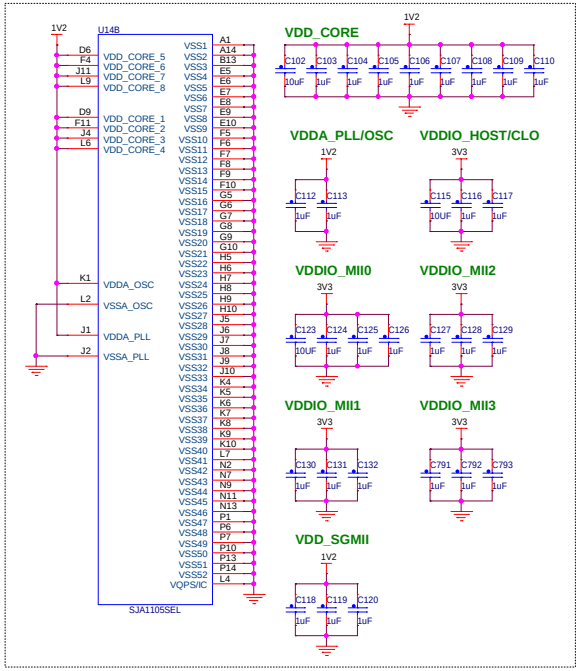
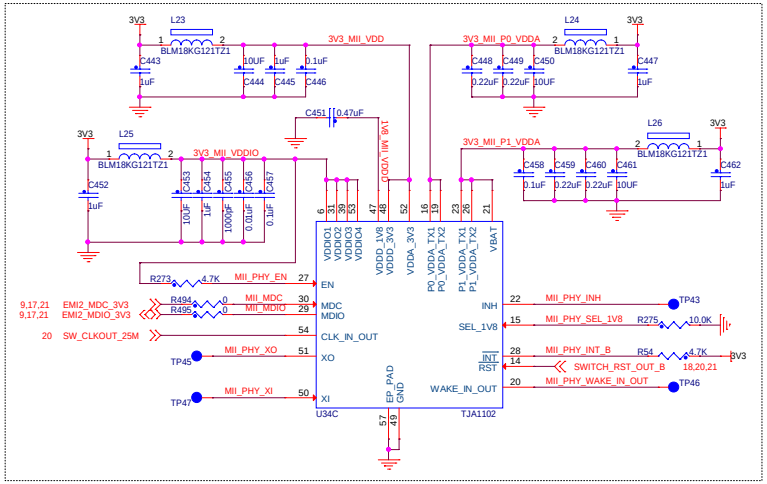
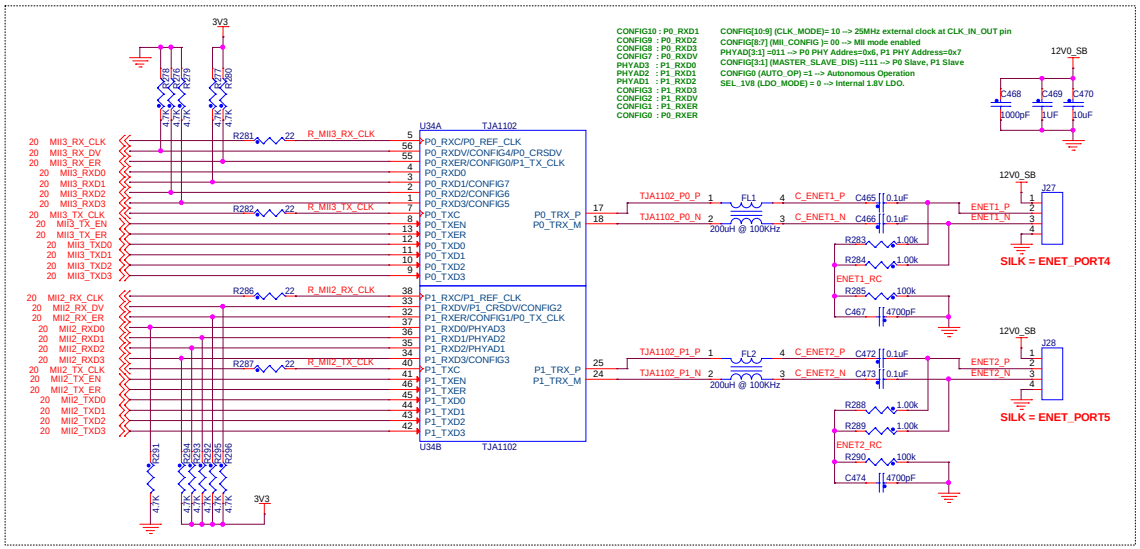
ETHERNET SWITCH & MII PHY









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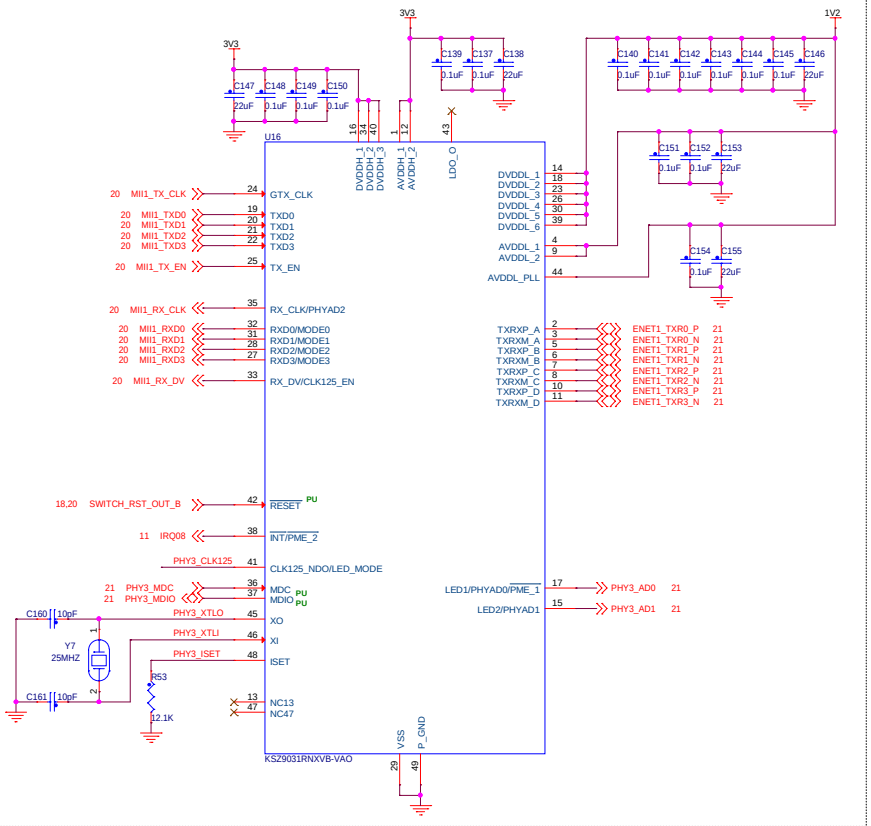
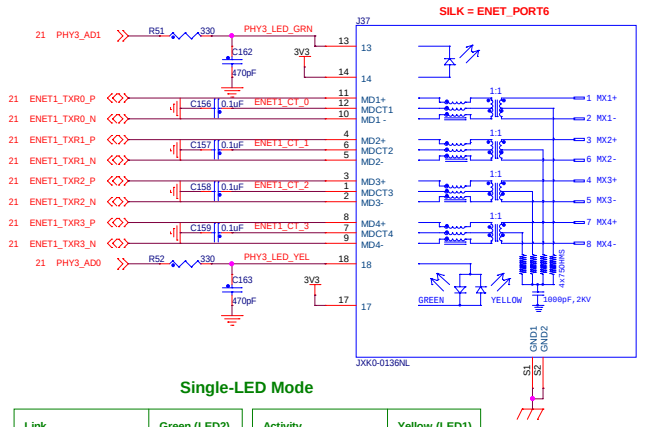
RGMII PHY#3

The recommended power-up sequence is to have the transceiver (AVDDH) and digital I/O (DVDDH) voltages power up before the 1.2V core (DVDDL, AVDDL, AVDDL_PLL) voltage.

There is no power sequence requirement between transceiver (AVDDH) and digital I/O (DVDDH) power rails.



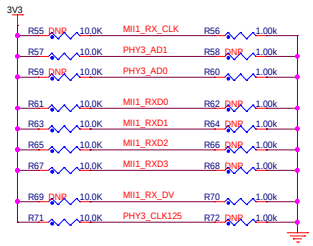


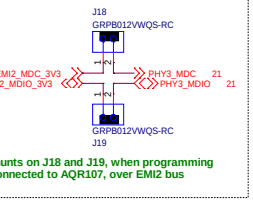
Single-LED Mode

Link	Green (LED2)
Link Off	OFF
Link On (any speed)	ON

Activity	Yellow (LED1)
No Activity	OFF
Activity (RX, TX)	Blinking

PIN	DESCRIPTION	DEFAULT CONFIGURATION
RX_CLK (PHYAD2) LED2 (PHYAD1) LED1 (PHYAD0)	PHY ADDRESS [2:0]:State of PHYADx Pins are latched into PHYCTRL register at system Hardware-Reset. Note PHY Address Bits [4:3] are always set to '00'	010
RXD3 (MODE3) RXD2 (MODE2) RXD1 (MODE1) RXD0 (MODE0)	0100 NAND tree 0111 Chip power-down 1100 RGMII,1000BT FD only 1101 RGMII,1000BT FD/HD only 1110 RGMII,all except 1000BT HD 1111 RGMII,all (10/100/1000 speed HD/FD) Others Reserved	1111
RX_DV (CLK125_EN)	1 = Enable 125 MHz clock output 0 = Disable 125 MHz clock output	0
CLK125_NDO (LED_MODE)	1 = Single-LED mode 0 = Tri-color dual-LED mode	1





Unmount shunts on J18 and J19, when programming SPI flash, connected to AQR107, over EMI2 bus

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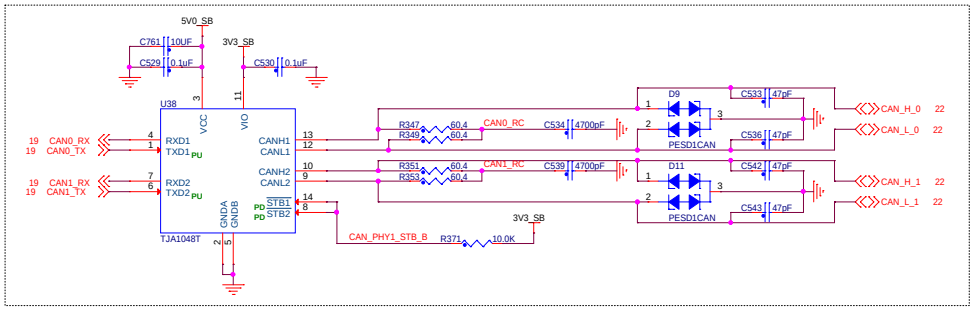
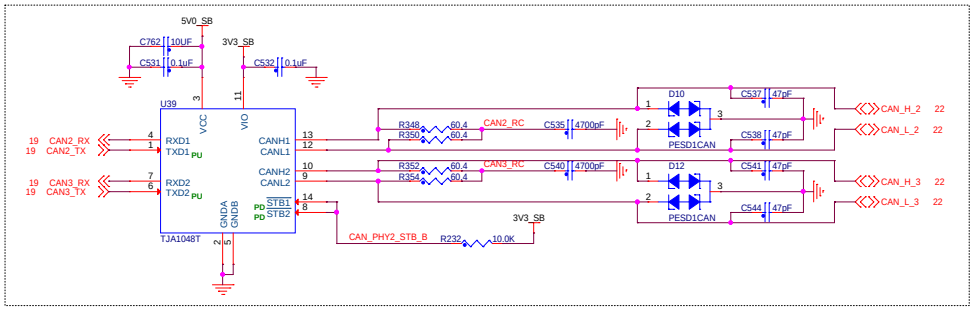
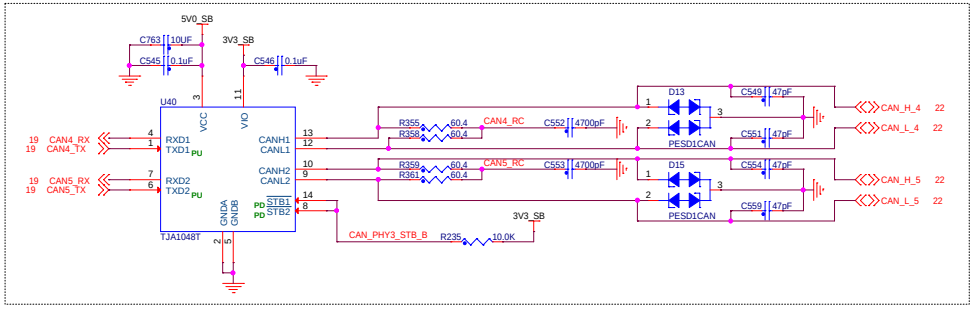
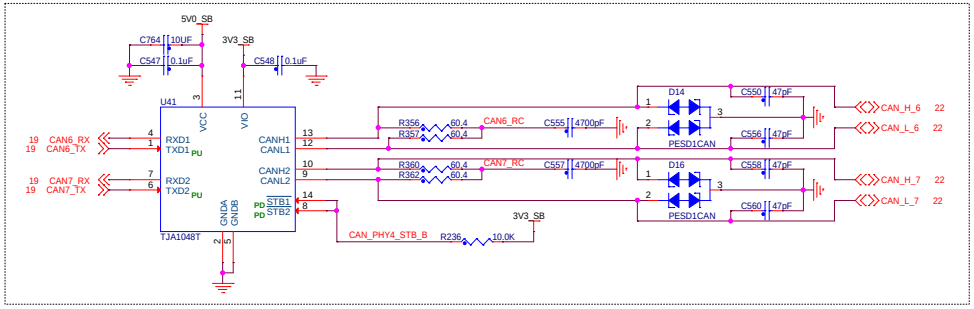
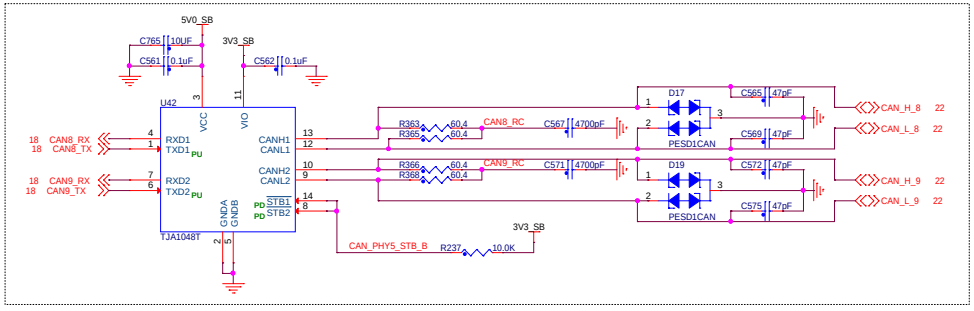
CAN PHY

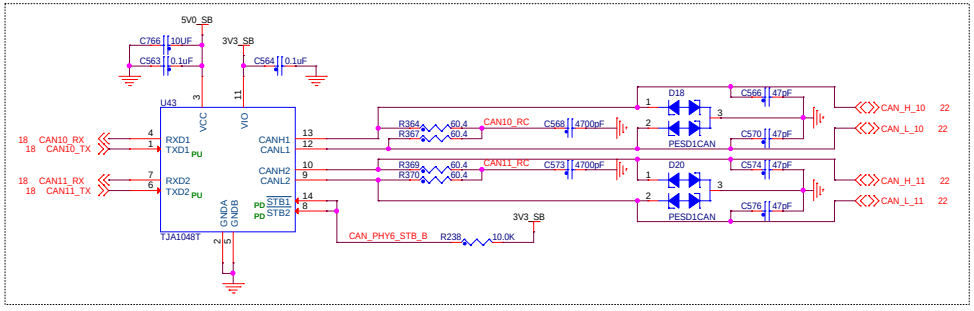




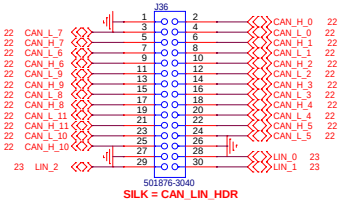








CAN[0:11] & LIN[0:2] CONNECTOR



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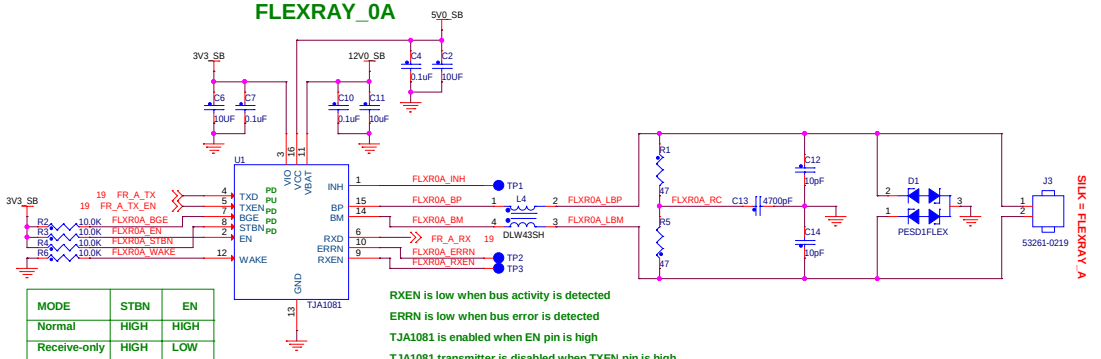
FLEXRAY & LIN

FLEXRAY_0A



MODE	STBN	EN
Normal	HIGH	HIGH
Receive-only	HIGH	LOW
Go-to-sleep	LOW	HIGH
Standby	LOW	LOW
Sleep	LOW	X

RXEN is low when bus activity is detected

ERRN is low when bus error is detected

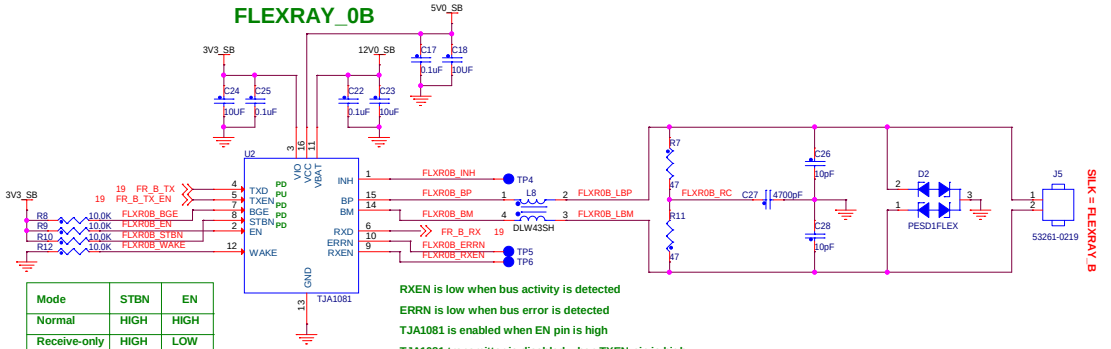
TJA1081 is enabled when EN pin is high

TJA1081 transmitter is disabled when TXEN pin is high

TJA1081 transmitter is disabled when BGE pin is low

TJA1081 enters low power mode when STBN pin is low

FLEXRAY_0B



Mode	STBN	EN
Normal	HIGH	HIGH
Receive-only	HIGH	LOW
Go-to-sleep	LOW	HIGH
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TJA1081 transmitter is disabled when TXEN pin is high

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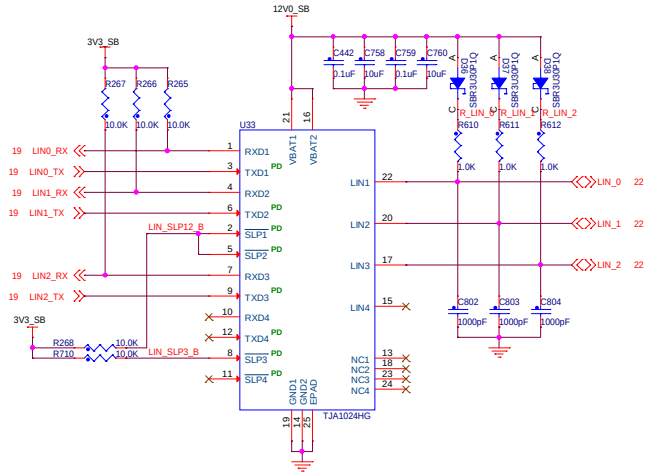
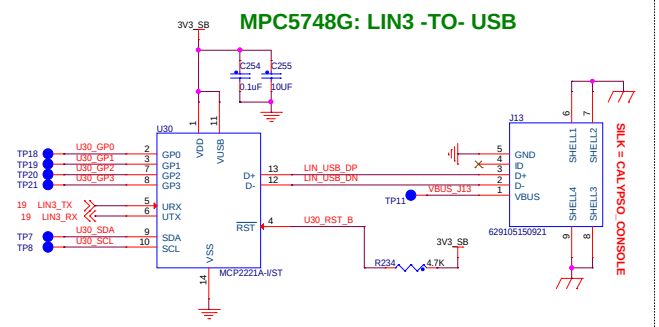
TJA1081 enters low power mode when STBN pin is low

LIN PHY



MPC5748G: LIN3 -TO- USB



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