

MPC5748G Gateway Evaluation Board (MPC5748G-GWEVB)

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Revision Information

| Rev | Date | Designer | Comments |
|-----|---------------|--------------|--|
| X1 | 24 March 2017 | Raymond Tang | Draft |
| A | 7 Jun 2017 | Raymond Tang | Final Release |
| B | 13 Dec 2017 | Raymond Tang | 1. Move net ON-OFF-CAN from PD0 to PD12 2. Move net ON-OFF-ETH from PD8 to PD13 3. Add pull-up resistors R503 & R504 on LIN RX 4. Remove R121, R175, R115 |
| C | 18 Jun 2018 | Raymond Tang | 1. Change U7 VBAT to 12V 2. Populate R189, R191, R194, R197 3. Add R505, R507-R510 4. Remove ADM6315 and add reset button SW1 on reset 5. Change connector type on page21 6. Change TJA1042T/3 to TJA1044GT/3 7. Change SJA1105TEL to SJA1105QEL |

Caution:

These schematics are provided for reference purposes only. As such, NXP does not make any warranty, implied or otherwise, as to the suitability of circuit design or component selection (type or value) used in these schematics for hardware design using the NXP Calypso family of Microprocessors. Customers using any part of these schematics as a basis for hardware design, do so at their own risk and NXP does not assume any liability for such a hardware design.

Notes:

- All components and board processes are to be ROHS compliant
- All small capacitors are 0603 unless otherwise stated
- All resistors are 0603 5% 0.1w unless otherwise stated. All zero ohm links are 0603
- All switches are denoted SWx
- All test points (SMT wire loop style) are denoted TPx
- Test point Vias (just through hole pads) are denoted TPVx

3 Different test points used in design:

TPVx - Through Hole Pad small

TPHx - Through Hole Pad Large (for standard 0.1" header). Also used on IO Matrix (IOMx)

TPx - Surface Mount Wire Loop

 TPV2


 TPH5

 TP?

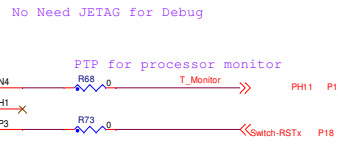
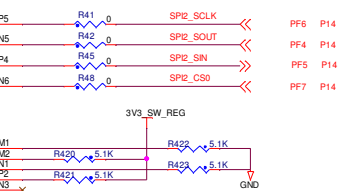
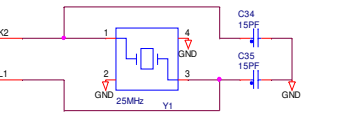
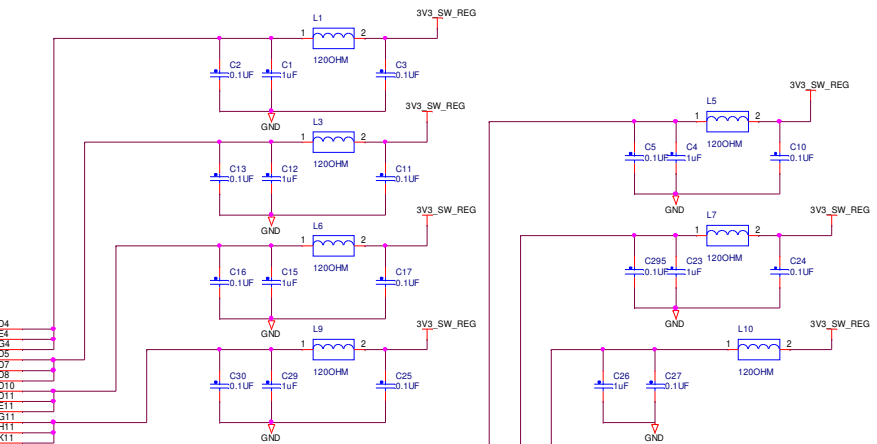
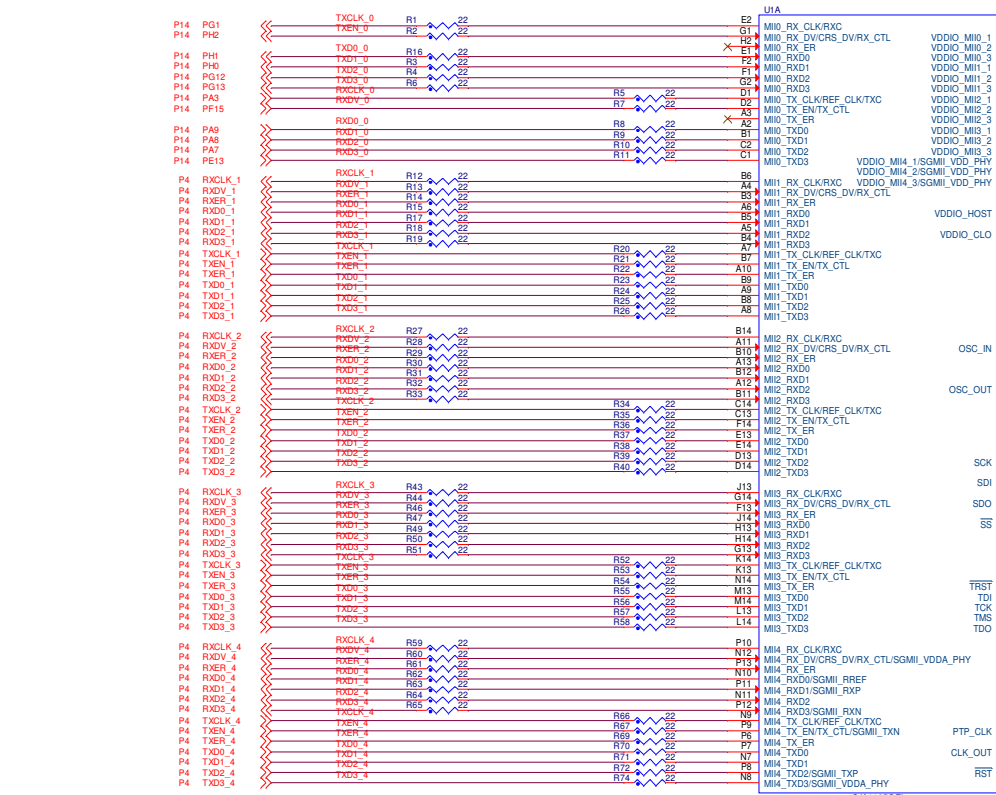
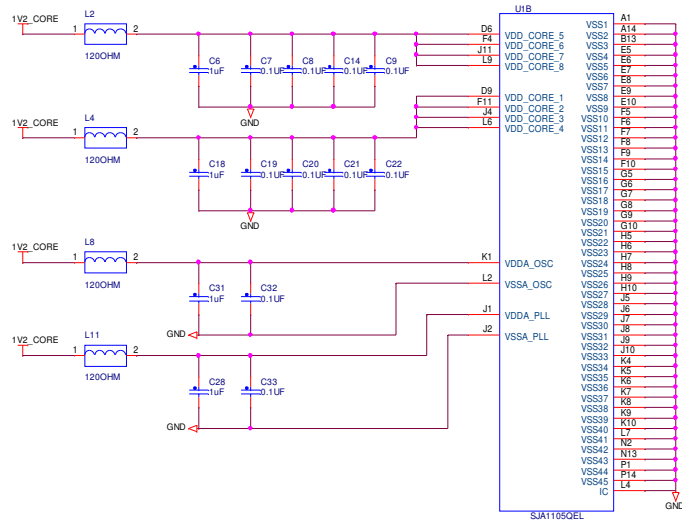
Signals (ports) have not been routed via busses as this makes it harder to determine where each signal goes.

User notes are given throughout the schematics.

Specific PCB LAYOUT notes are detailed in LCD

| | | | |
|--|-----------|--|----------|
|  | | Automotive Product Group 6501 William Cannon Drive West Austin, TX 78755-8500 | |
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| Designer: Raymond Tang | | Drawing Title: MPC5748G-GW | |
| Drawn by: Raymond Tang | | Page Title: Index and Title Page | |
| Approved: Raymond Tang | Size C | Document Number SCH-29810 PDF-SPF-29810 | Rev C |
| Date: Friday, June 22, 2018 | | Sheet 1 of 21 | |

Ethernet Switch (Configured for MII Mode)



SPI2 with Processor

No Need JETAG for Debug

PTP for processor monitor

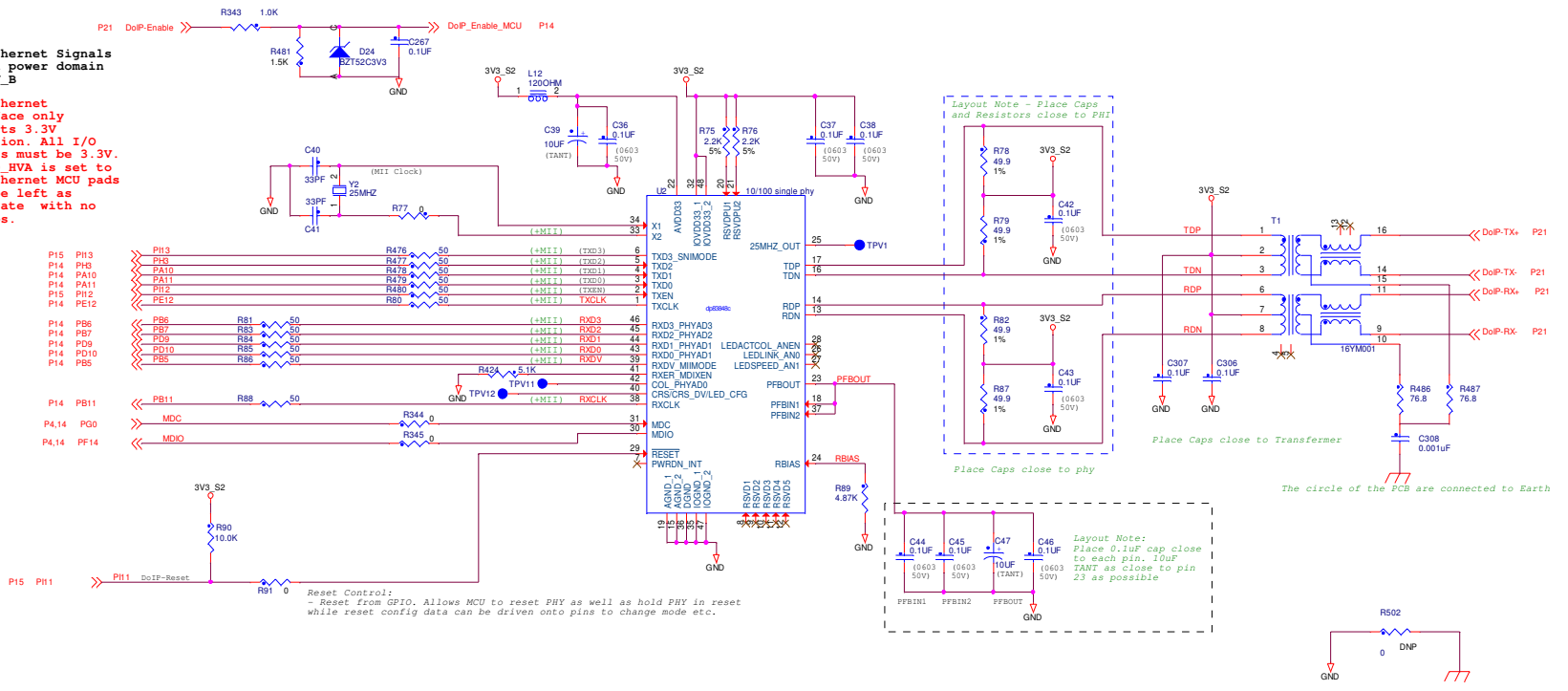


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| ICAP Classification: CP | | LUD | | PUB: | |
| Drawing Title: MPC5748G-GW | | | | | |
| Page Title: Ethernet Switch | | | | | |
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Ethernet Diag

All Ethernet Signals are in power domain VDD_HV_B

The Ethernet interface only supports 3.3V operation. All I/O signals must be 3.3V. If VDD_HVA is set to 5V, Ethernet MCU pads must be left as tri-state with no pullups.



Boot Configuration (using PHY internal Pulls)

- Auto Negotiation Enable (All speeds / duplex supported) (AN_EN, AN0 and AN1 all Internal PullUp)
- Operating Mode (MII or RMII) (SMT_Mode Internal PullDown, MII_Mode control via jumper)
- LED Configuraiton (Model) (LED_CFG Internal PullUp)
- MDIX Enable (Auto MDIX Enabled) (MDIX_EN Internal PullUp)
- Physical Address (set to 0b000001) (PHYAD[0] Internal PullUp, PHYAD[1..4] Internal PullDown)

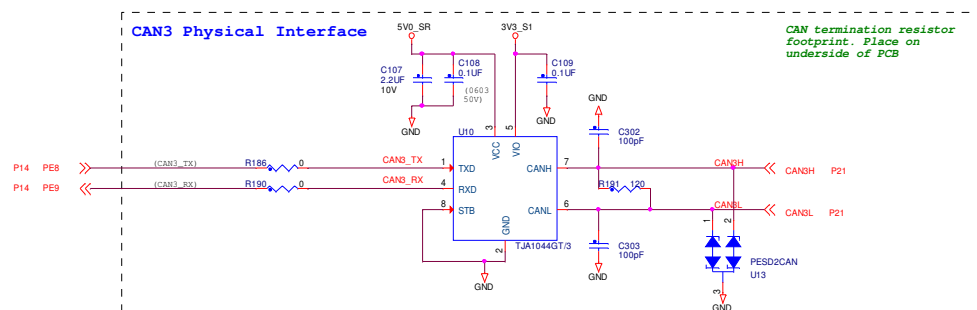
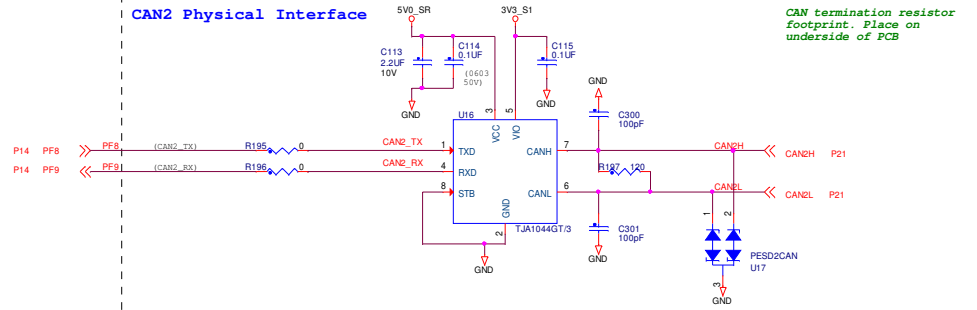
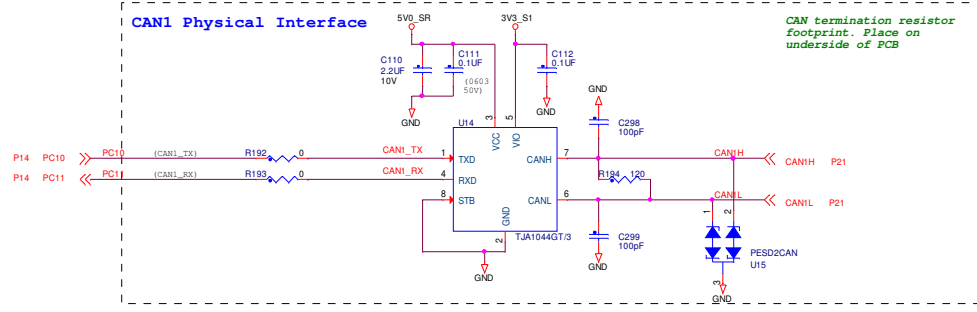
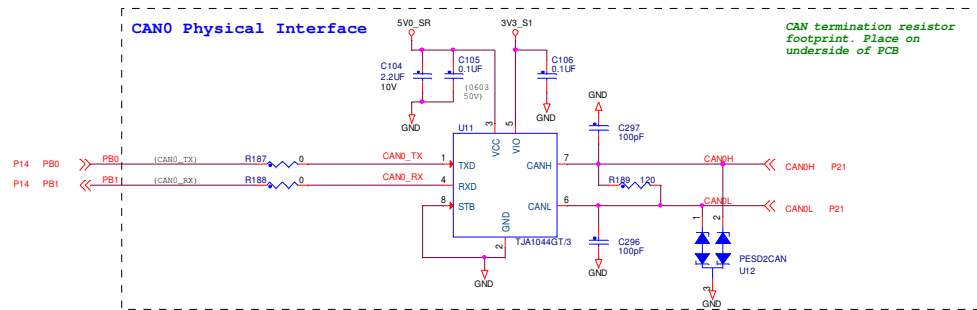
Layout Note:
MII Mode resistor (MII / RMII mode) and the MDIO ullup resistor should be placed as close as possible to the PF15 / PF14 tracks to reduce the effect of a stub on the transmission line.

ICAP Classification: CP: IJO: PJB:

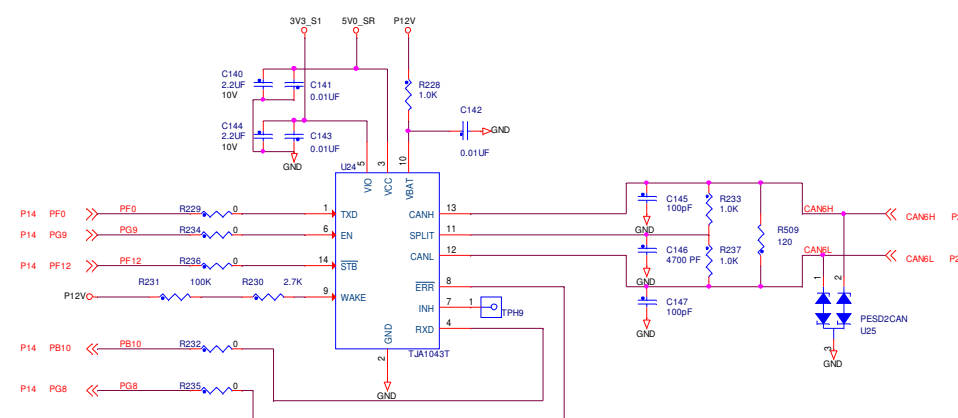
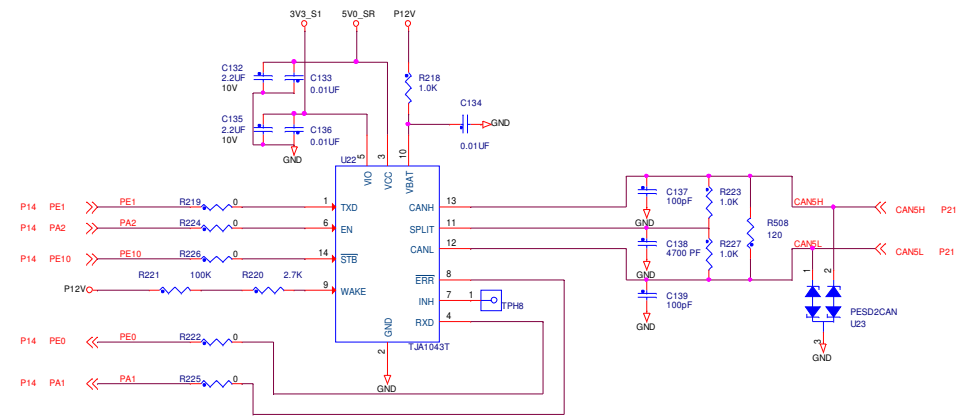
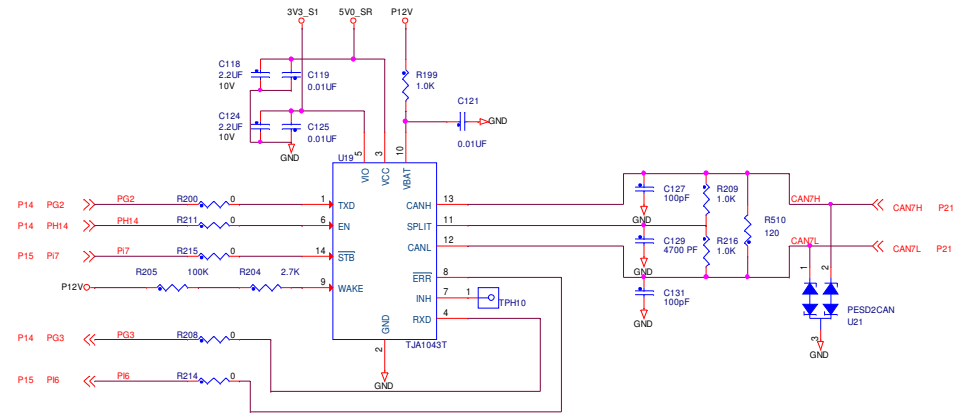
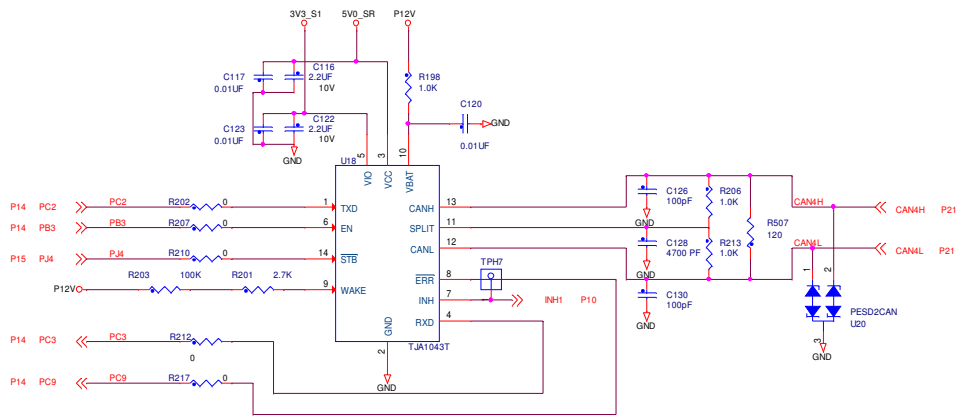
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Page Title: **Ethernet Diag**

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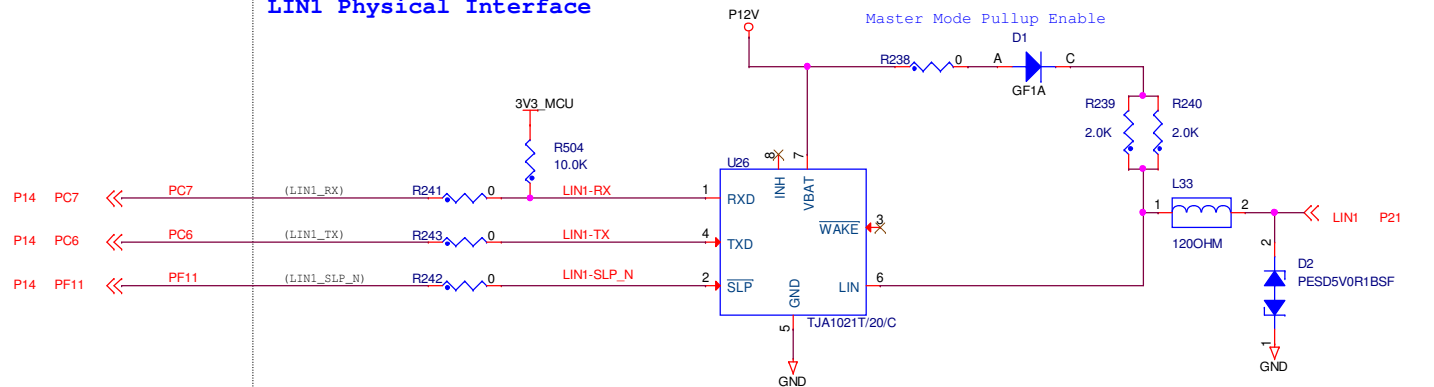


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| Page Title: | | | | |
| CAN | | | | |
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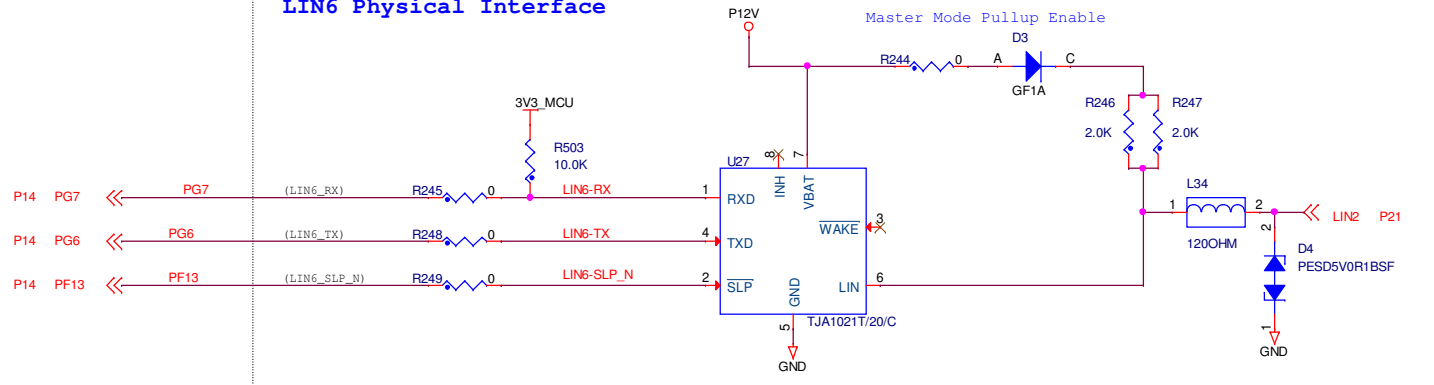


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| Page Title: | | CAN2 | |
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LIN1 Physical Interface



LIN6 Physical Interface



ICAP Classification: CP: IUO: PUBI:

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MPC5748G-GW

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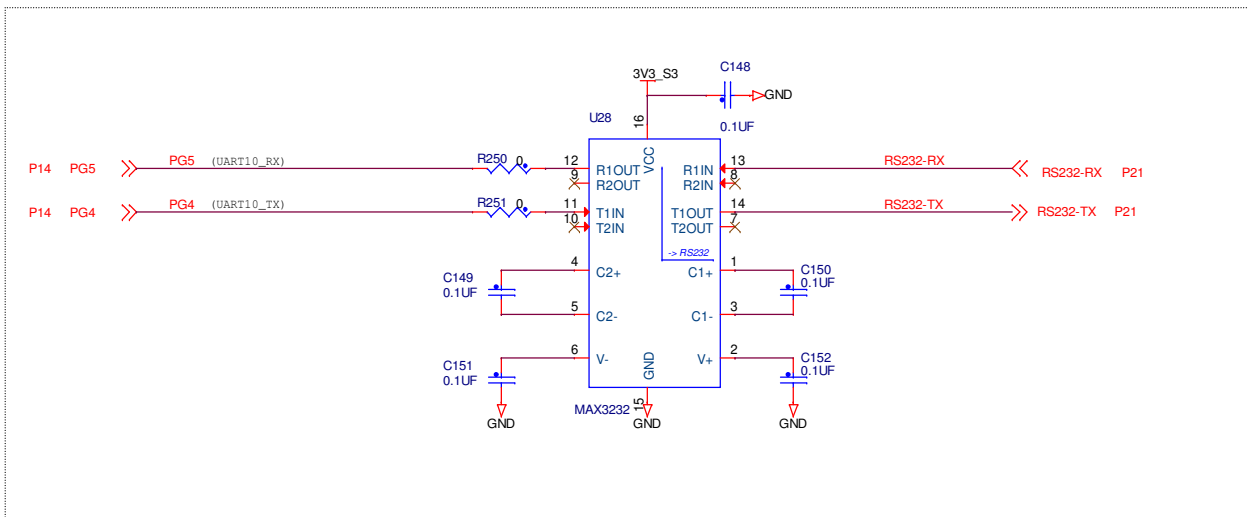
LIN

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| Size | Document Number | SCH-29810 | PDF: SPF-29810 | Rev C |
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RS232

RS232 for debug



ICAP Classification: CP: IUC: PUBI:

Drawing Title:

MPC5748G-GW

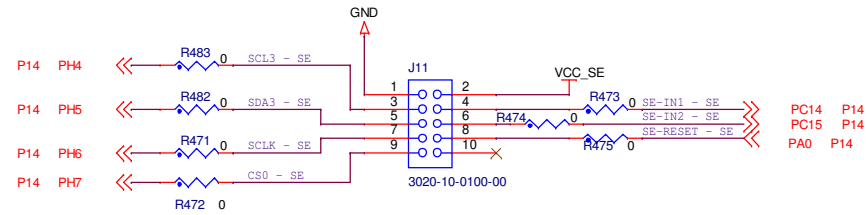
Page Title:

RS232

| Size | Document Number | Rev |
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| | SCH-29810 PDF: SPF-29810 | C |

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Security Element



ICAP Classification: CP: IUO: PUBI:

Drawing Title:

MPC5748G-GW

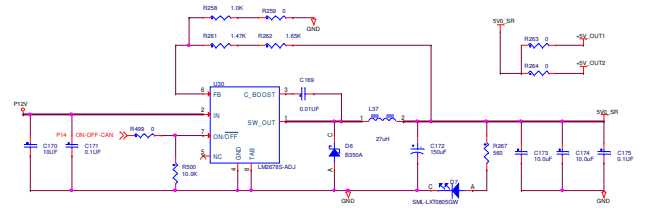
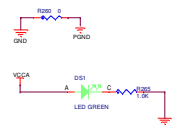
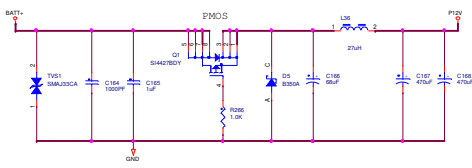
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Security Element

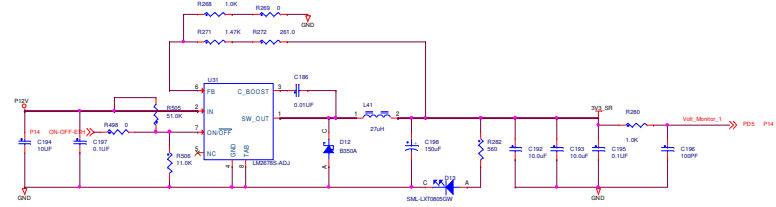
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| Size | Document Number | SCH-29810 | PDF: SPF-29810 | Rev C |
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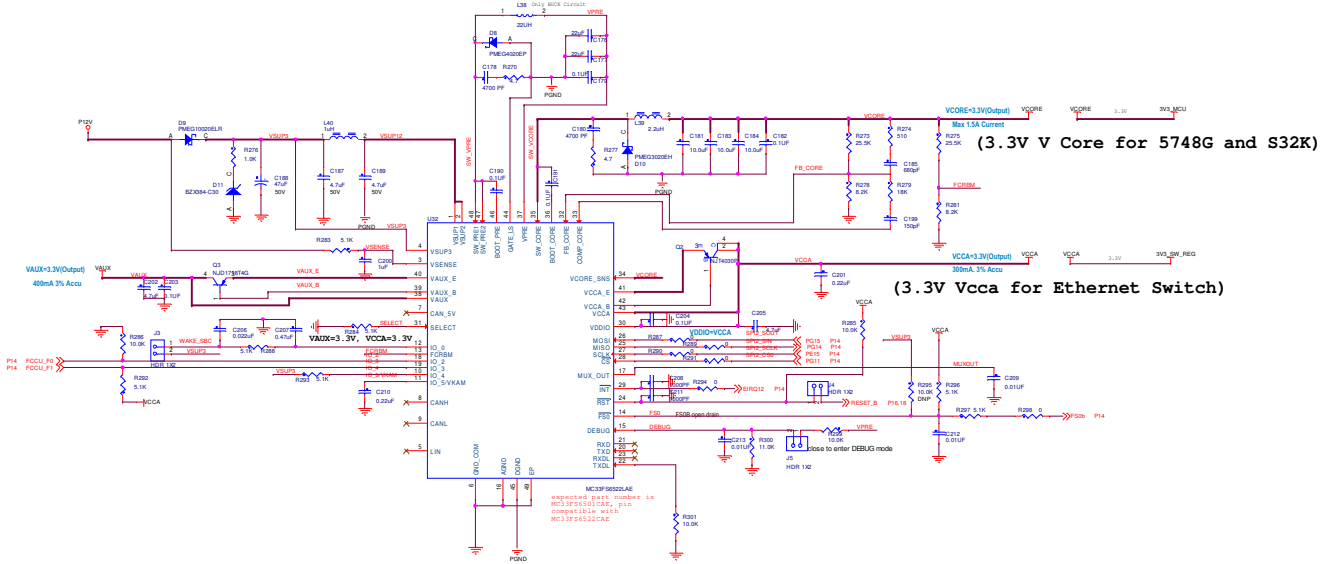
Power Supply



(12V input, 2.0A Output, 89% Efficient, for CAN, DoIP etc)

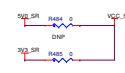


(12V input, 2.0A Output, 83% Efficient, for Ethernet PHY)

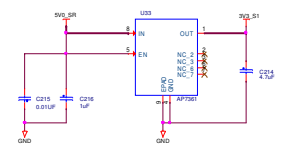


(3.3V V Core for 5748G and S32K)

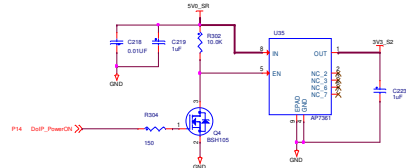
(3.3V Vcca for Ethernet Switch)



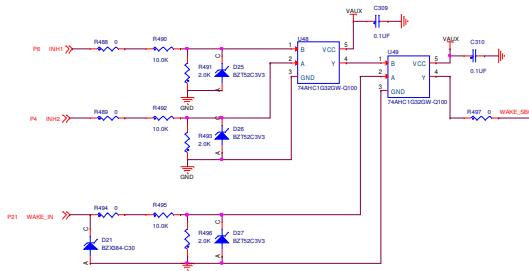
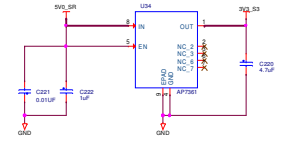
(5V Input, 3.3V output, for eMMC, CAN-VIO)



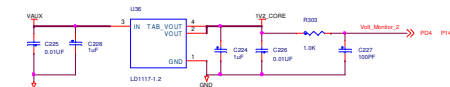
(5V Input, 3.3V output, for FlexRay, Rs232)



(5V Input, 3.3V output, for DoIP Ethernet Phy)



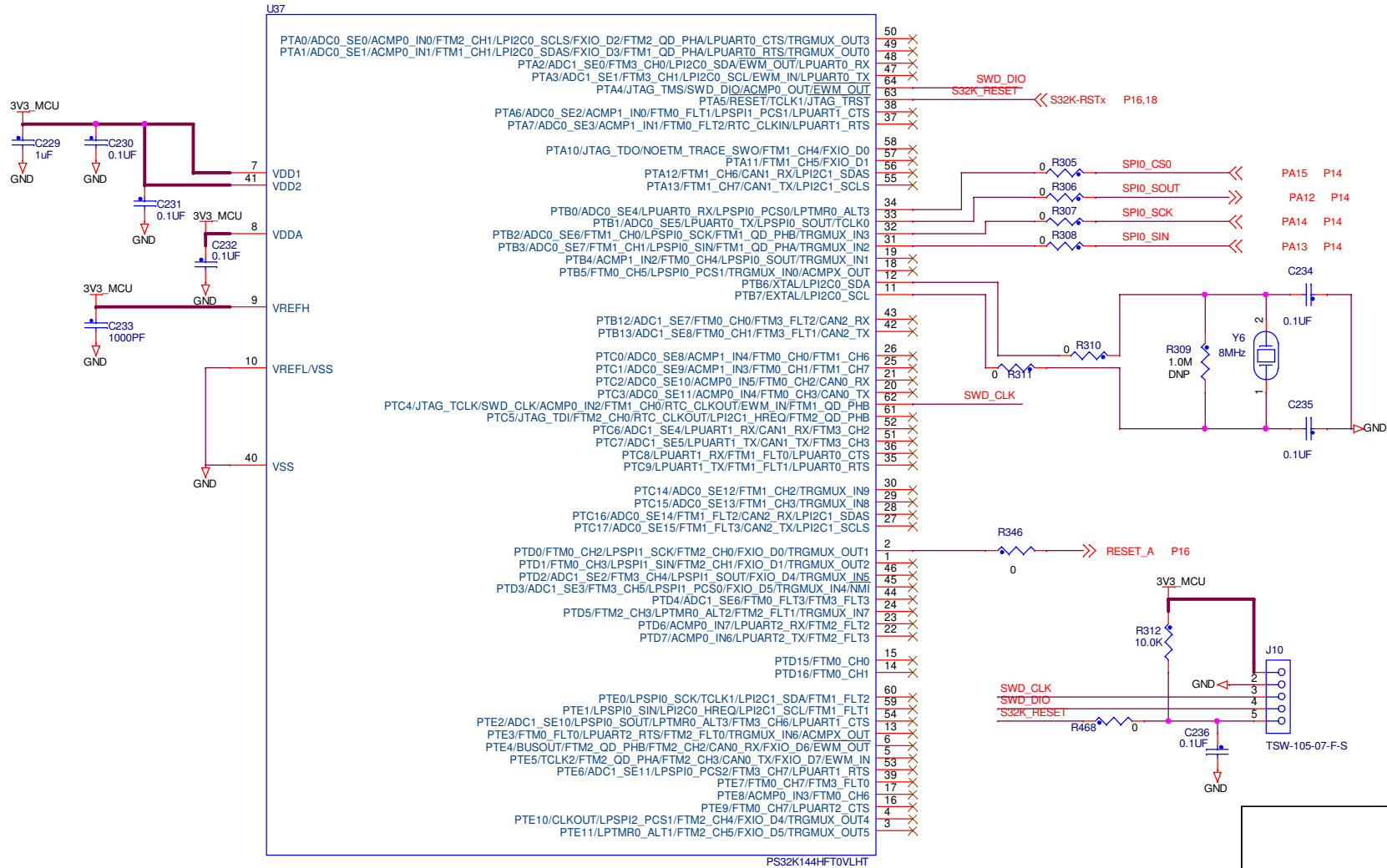
(Wakeup network for SBC)



(3.3V Input, 1.2V Output for Ethernet Switch)

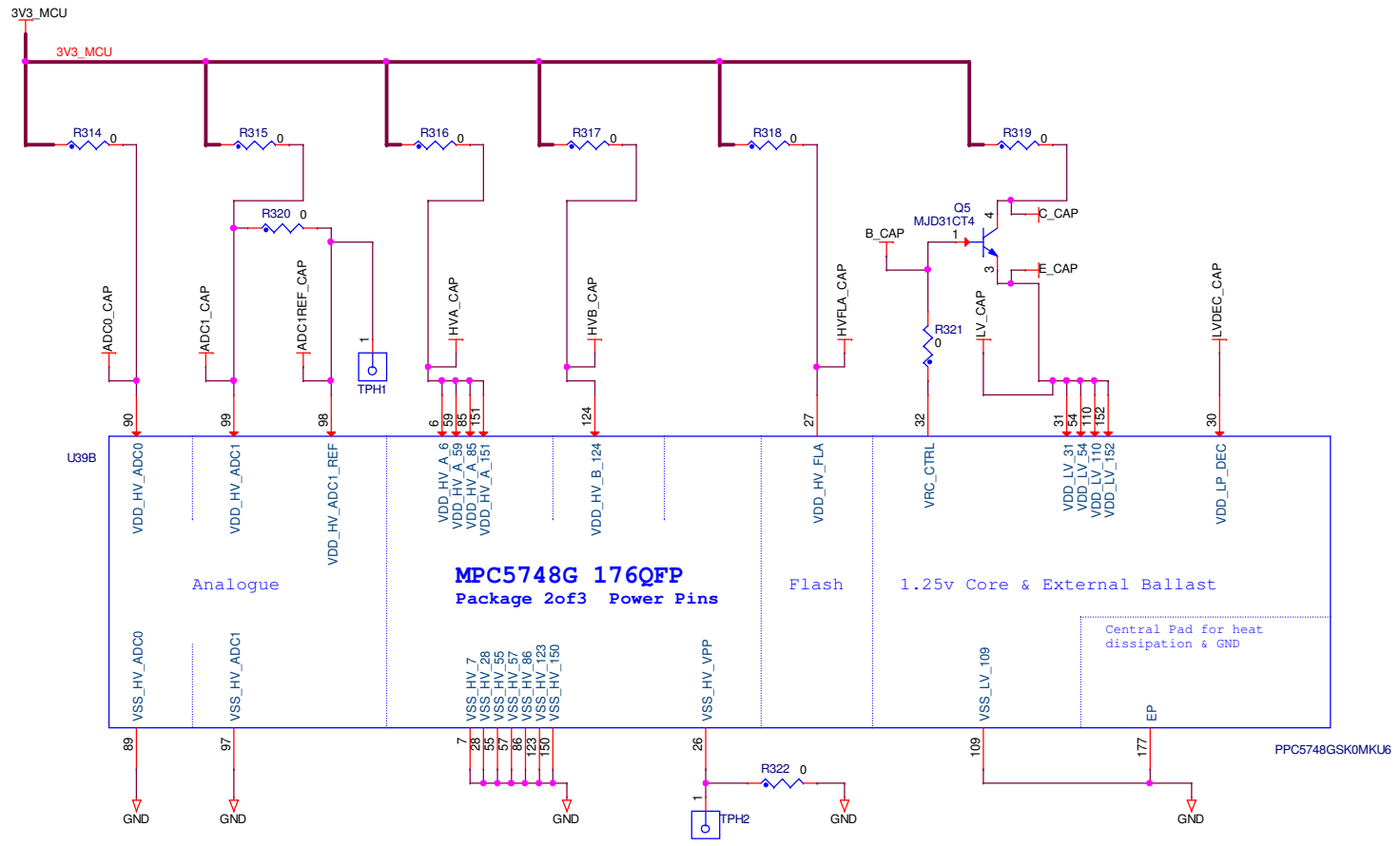
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| ICAP Organization: | QP | SD | X PWR |
| Drawing Title: | MPC5748G-GW | | |
| Page Title: | POWER SUPPLY | | |
| Rev D | Document Number: | SCH28810 PDF: SPF28810 | Rev C |
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S32K MCU



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| ICAP Classification: | | CP: | IUC: | PUBI: |
| Drawing Title: | | | | |
| MPC5748G-GW | | | | |
| Page Title: | | | | |
| S32K MCU | | | | |
| Size | Document Number | SCH-29810 PDF: SPF-29810 | | Rev C |
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MPC5748G MCU Power Connections



Notes on signal Grounds:

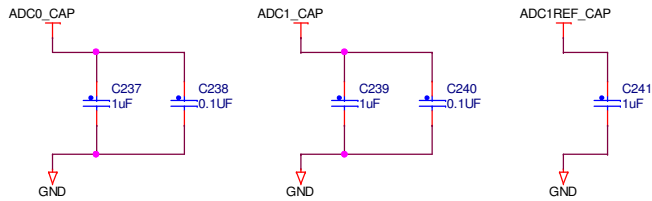
- The scheme shown has the analogue and digital grounds connected to the same plane
- This results in better ADC performance than using an analogue ground plane with single entry point (or ferrite) to digital ground plane.



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| ICAP Classification: | | CP: | IUC: | PUBI: |
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| MPC5748G-GW | | | | |
| Bage Title: | | | | |
| Calypso MCU Power | | | | |
| Size | Document Number | SCH-29810 | PDF: SPF-29810 | Rev C |
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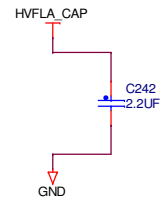
MPC5748G MCU Decoupling and bulk storage

ADC



Place small Caps as close as possible to MCU pins

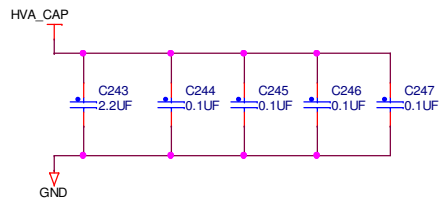
Flash



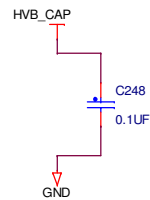
Capacitor Types:

- 4700pF - Ceramic X7R, 50V 10% 0402
- 0.1uF - Ceramic X7R, 16V 10% 0402 (Kemet C0402C104K4RAC)
- 0.68uF - Ceramic X7R, 16V 10% 0805 (Murata GCM219R71C684KA37)
- 1uF - Ceramic X7R, 10V 10% 0603 Low ESR (Taiyo Yuden LMK107B7105KA-T)
- 2.2uF - Ceramic X7R, 10V 10% 0603 Low ESR (Taiyo Yuden LMK107B7225KA-TR)

VDD_HVA

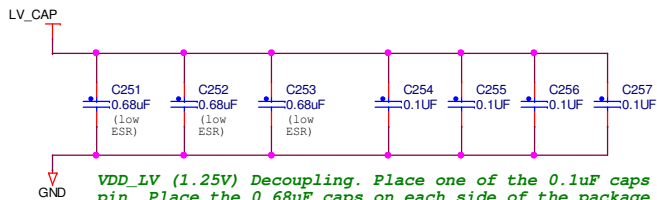


VDD_HVB



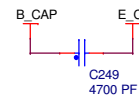
One 0.1uF cap per VDD_HV_x pin. Place as close as possible to pin

VDD_LV



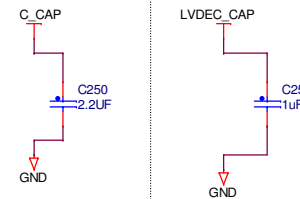
VDD_LV (1.25V) Decoupling. Place one of the 0.1uF caps close to each VDD_LV pin. Place the 0.68uF caps on each side of the package such that there is no cap on the side with the ballast transistor (For regulator stability the total capacitance should be around 2.2uF).

Ballast Transistor



Place close to transistor

LP Internal Reg Cap



ICAP Classification: CP: IUO: PUBI:

Drawing Title:

MPC5748G-GW

Page Title:

Calypso MCU Decoupling

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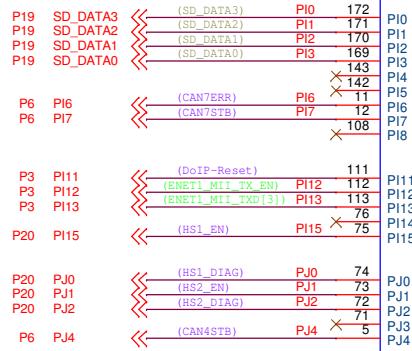
U89A

Key to text colours:
 Purple - Comms Physical Interfaces
 Orange - Other Peripherals and I/O
 Blue - Debug (JTAG)
 Black - Clock, Reset and Control
 RED - I/O Matrix and other functions (eg LED)
 Green - I/O Matrix (dedicated)

| | | | | |
|-----|------|---------------------|-------|-----|
| P9 | PA0 | SE-RESET - SE | PA0 | 24 |
| P6 | PA1 | (CANSERR) | PA1 | 19 |
| P6 | PA2 | (CANSER) | PA2 | 17 |
| P2 | PA3 | (ENET0_MII_RX_CLK) | PA3 | 114 |
| P4 | PA4 | (WKP09) | PA4 | 51 |
| P18 | PA5 | (RESET_EthernetPhy) | PA5 | 146 |
| | | | PA6 | 147 |
| | | | PA7 | 128 |
| P2 | PA7 | (ENET0_MII_RXD[2]) | PA7 | 128 |
| P2 | PA8 | (ENET0_MII_RXD[1]) | PA8 | 129 |
| P2 | PA9 | (ENET0_MII_RXD[0]) | PA9 | 130 |
| P3 | PA10 | (ENET1_MII_TXD[1]) | PA10 | 131 |
| P3 | PA11 | (ENET1_MII_TXD[0]) | PA11 | 132 |
| P11 | PA12 | (SPI0_SIN) | PA12 | 53 |
| P11 | PA13 | (SPI0_SOUT) | PA13 | 52 |
| P11 | PA14 | (SPI0_CS) | PA14 | 50 |
| P11 | PA15 | (SPI0_CLK) | PA15 | 48 |
| | | | PA16 | 49 |
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MPC5748G GPIO 2 of 2

Key to text colours:
 Purple - Comms Physical Interfaces
 Orange - Other Peripherals and I/O
 Blue - Debug (JTAG & Nexus)
 Black - Clock, Reset and Control
 RED - I/O Matrix and other functions (eg LED)
 Green - I/O Matrix (dedicated)



U39C

PPC5748GSK0MKU6

MPC5748G 176QFP
 Package 3of3 GPIO Pins2



ICAP Classification: CP: IUC: PUBI:

Drawing Title:

MPC5748G-GW

Page Title:

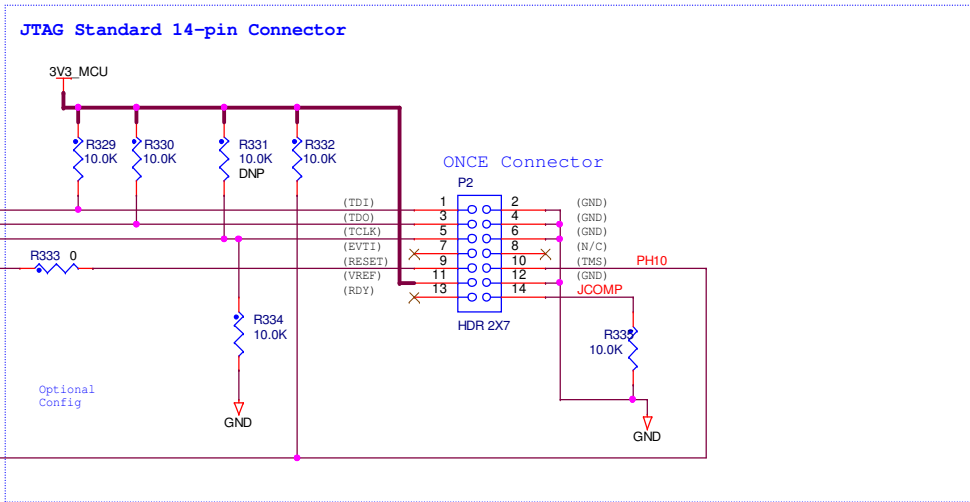
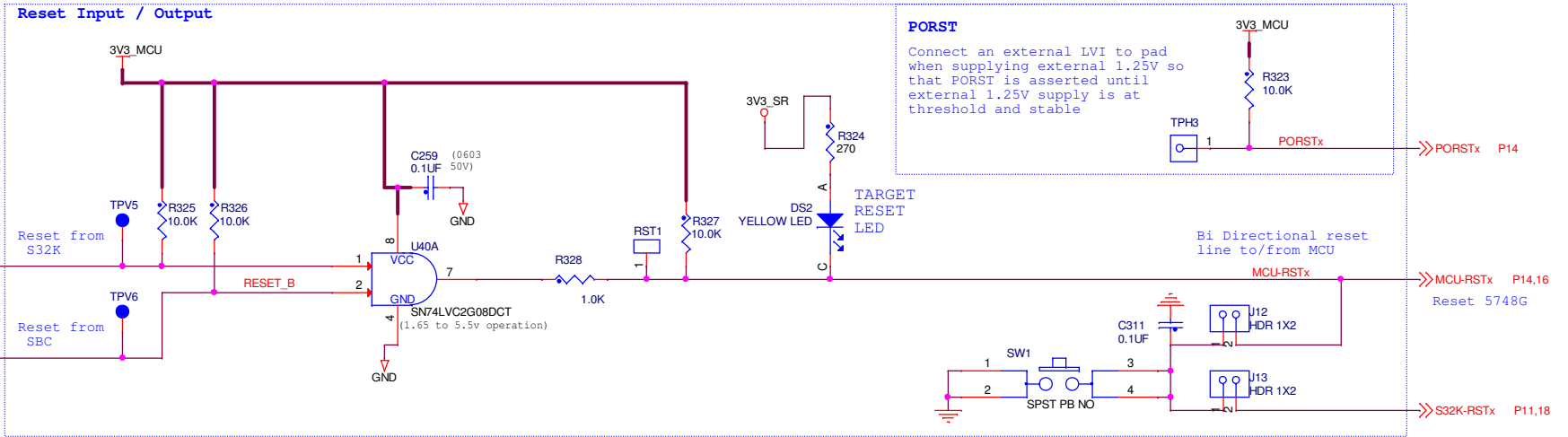
Calypso GPIO 2of2

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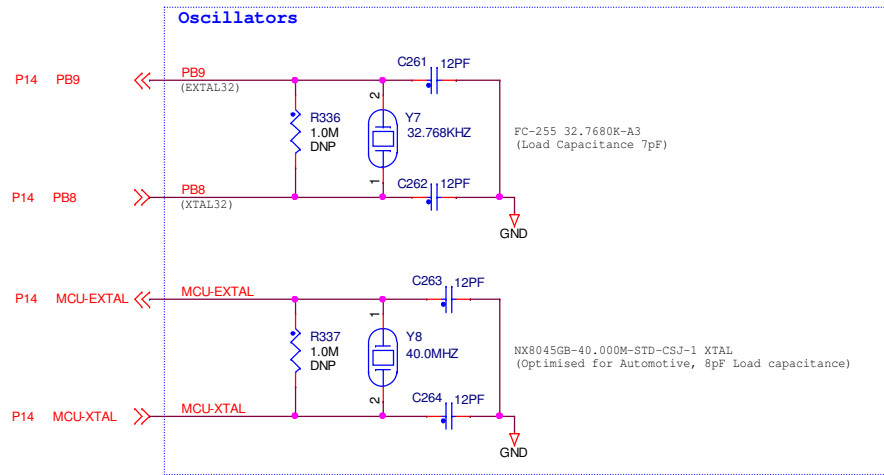
Reset

Reset is in the VDD_HVA domain.



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| Drawing Title: MPC5748G-GW | | | |
| Page Title: Calypso Reset and JTAG | | | |
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Clocks



ICAP Classification: CP: IUO: PUBI:

Drawing Title:

MPC5748G-GW

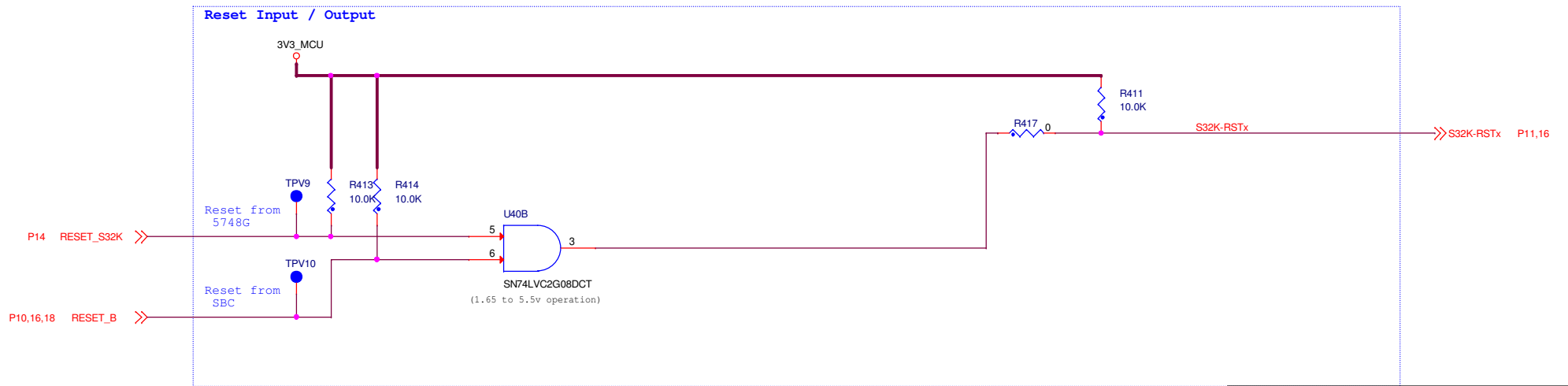
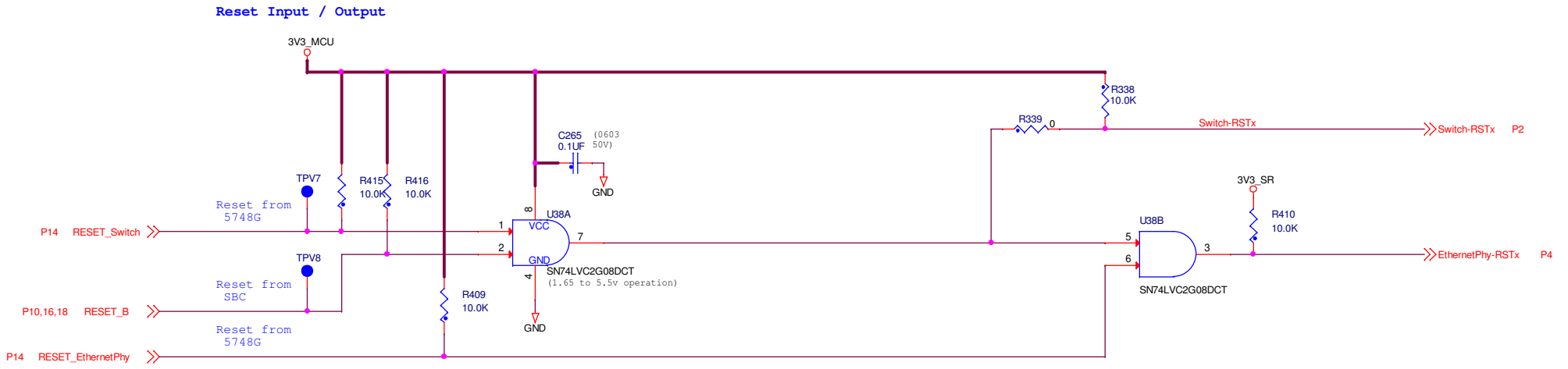
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Calypso Clocks

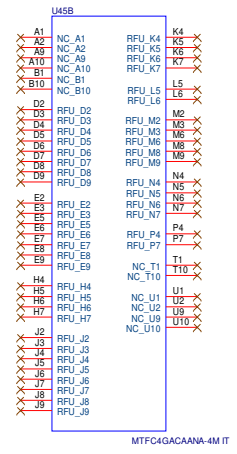
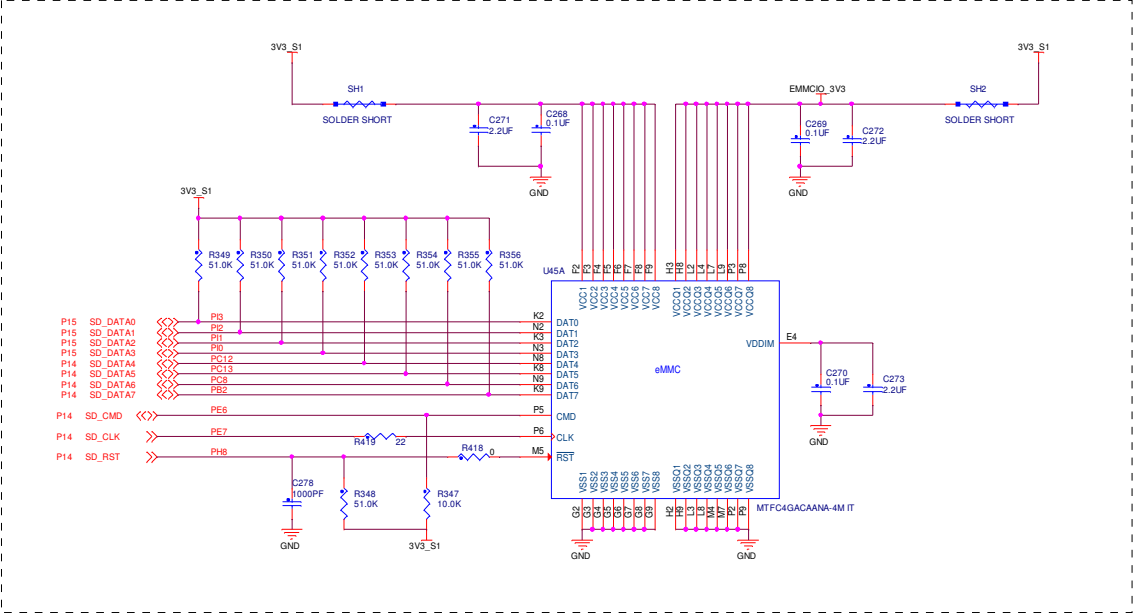
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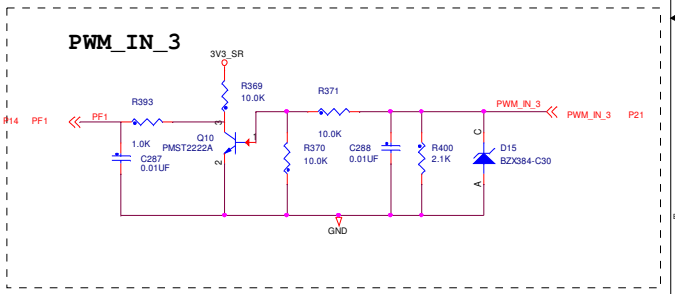
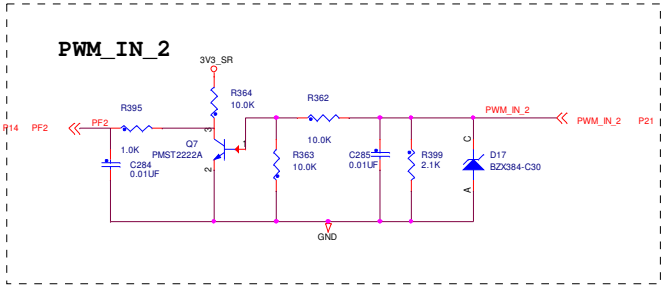
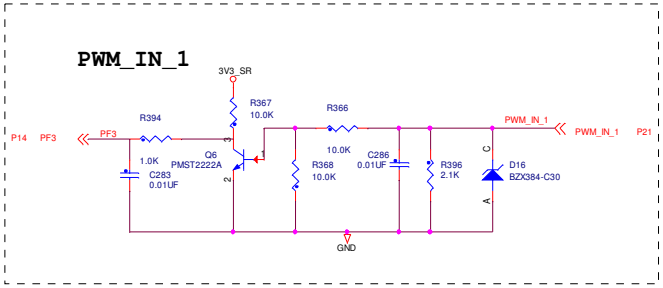
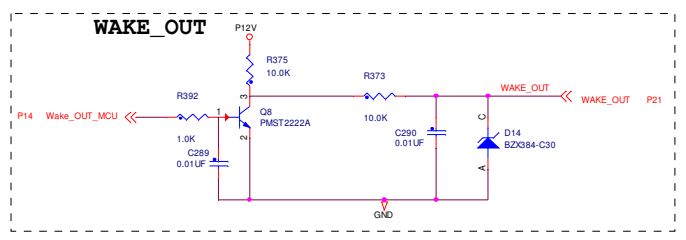
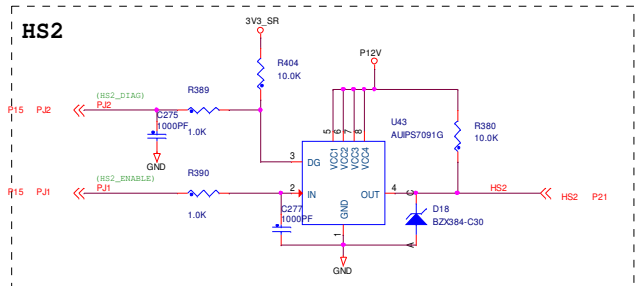
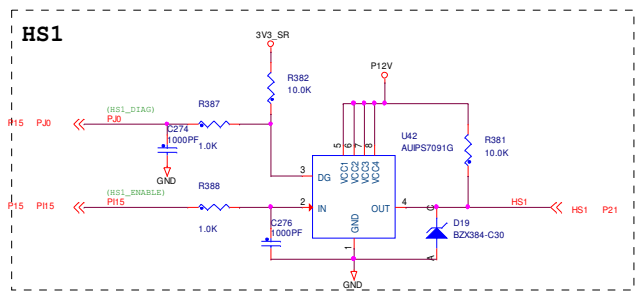
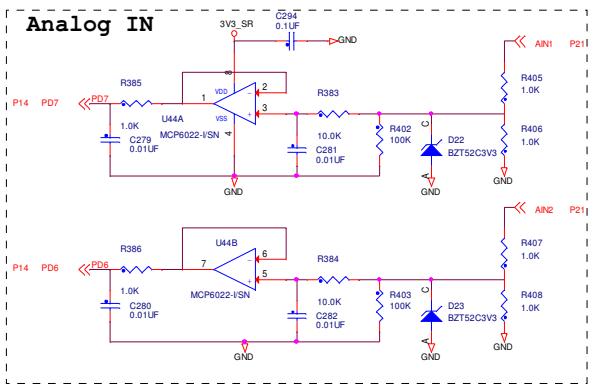
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Reset

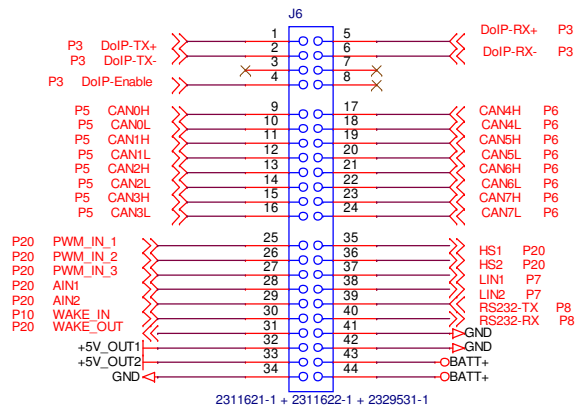
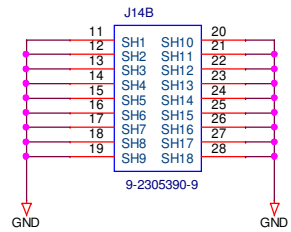
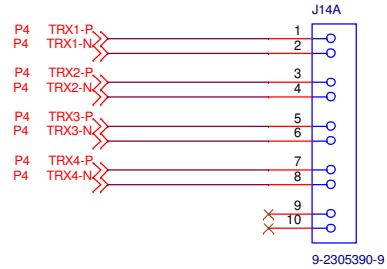


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Connector



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Drawing Title:

MPC5748G-GWEVB

Page Title:

Connector

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