

Nikhil Menon

ABSTRACT

This User's Guide discusses how to properly operate and configure the DP83561EVM. For best layout practices, schematic files, and Bill of Materials, see the associated sections and support documents.

DP83561EVM consists of a main PCB and two breakout boards: DP83561-SP Ethernet board, MAC interface breakout board, and MAC interface back-to-back connector.

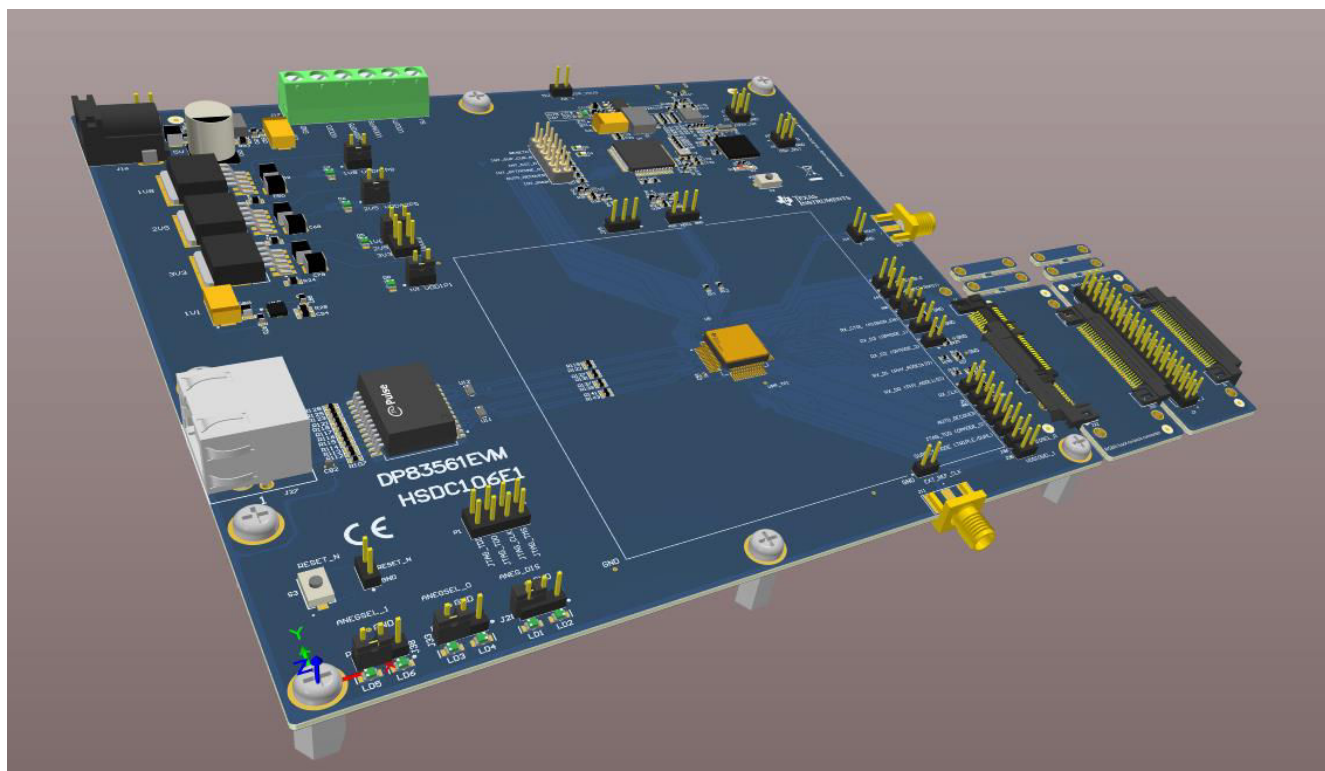


Figure 1-1. DP83561EVM Main PCB and Two Breakout Boards

2.2 Block Diagram

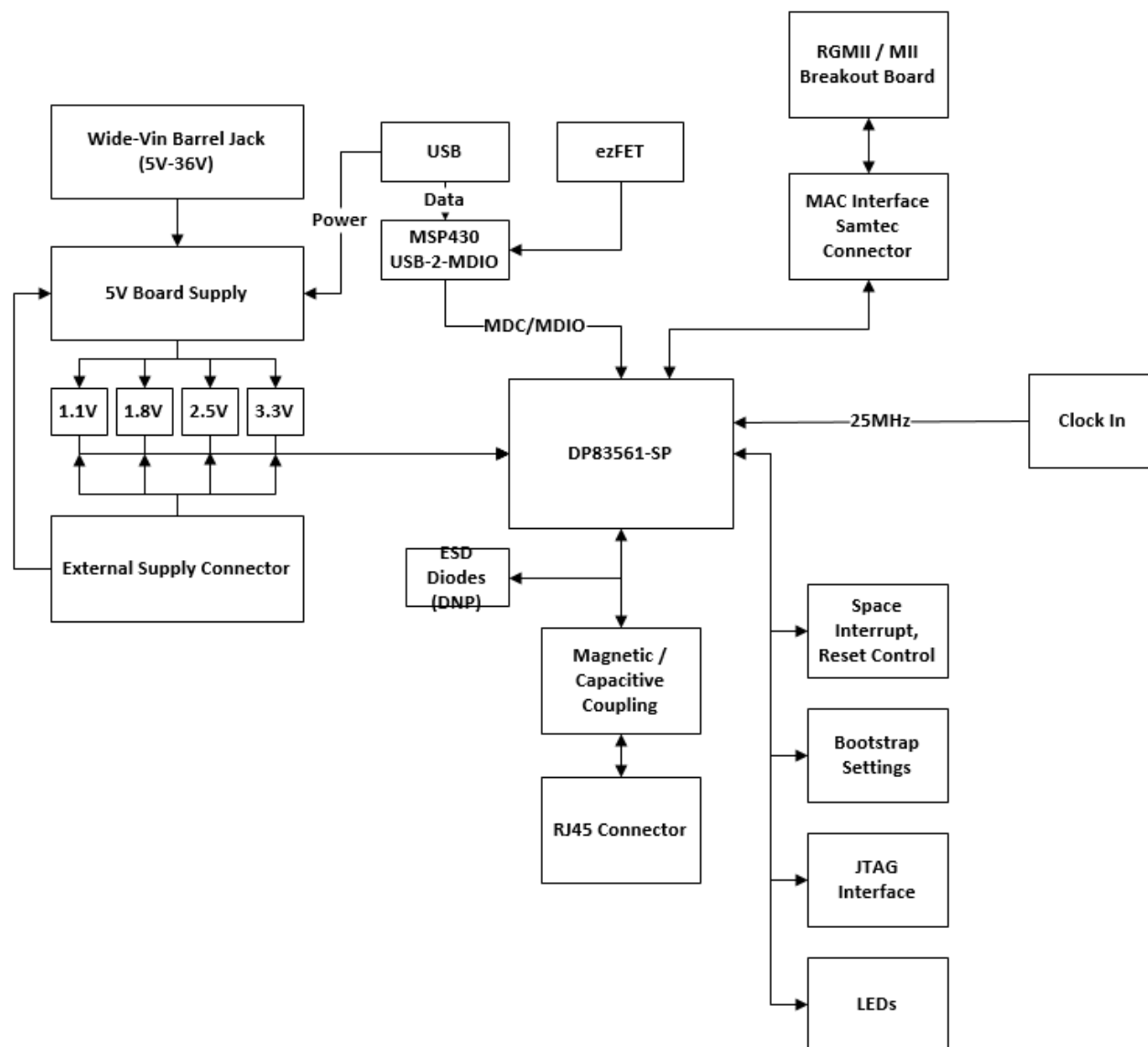


Figure 2-3. DP83561EVM Block Diagram

8 Schematics

8.1 Main Power Schematic

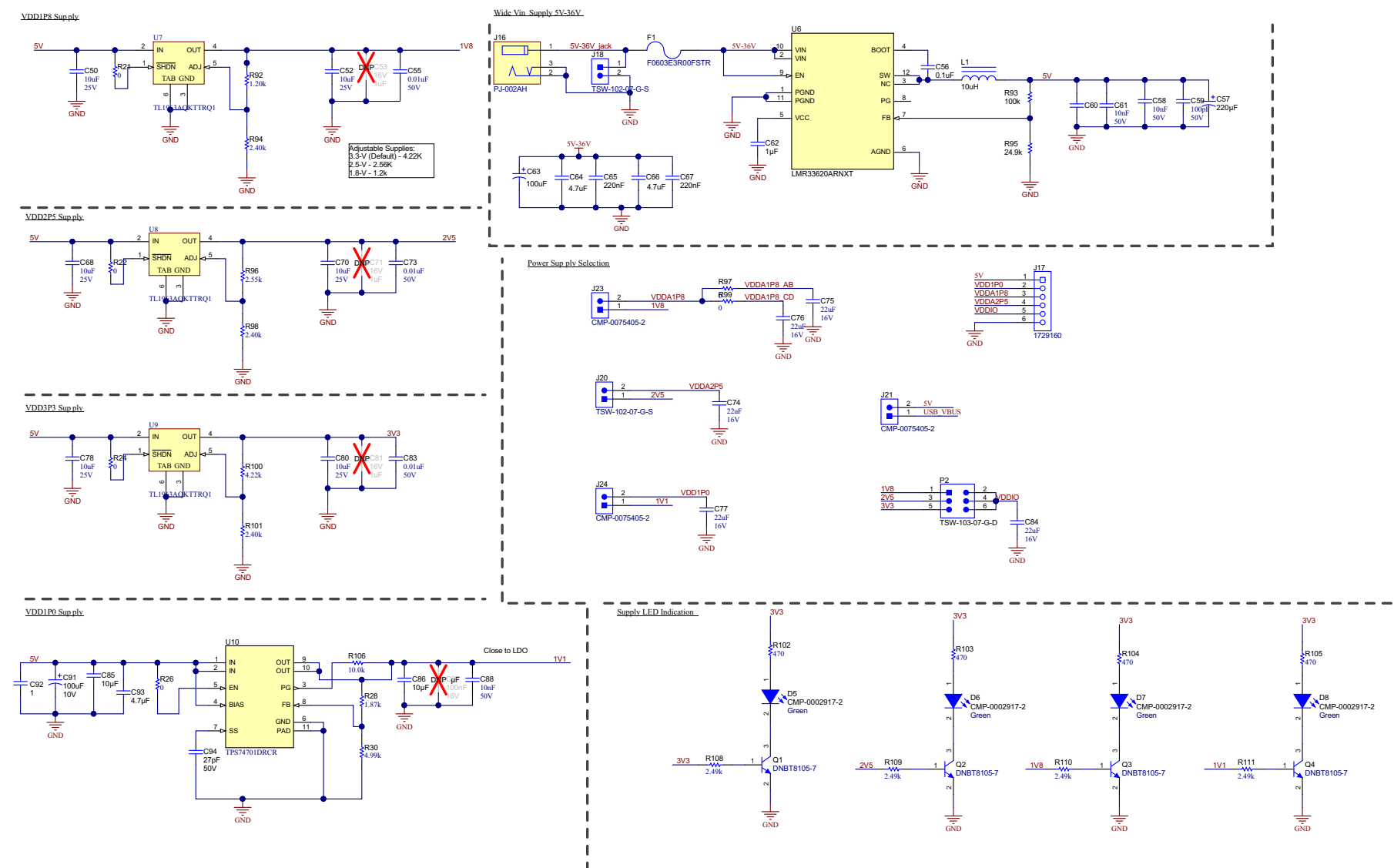


Figure 8-1. DP83561EVM Main Power

8.2 Main Block Schematic

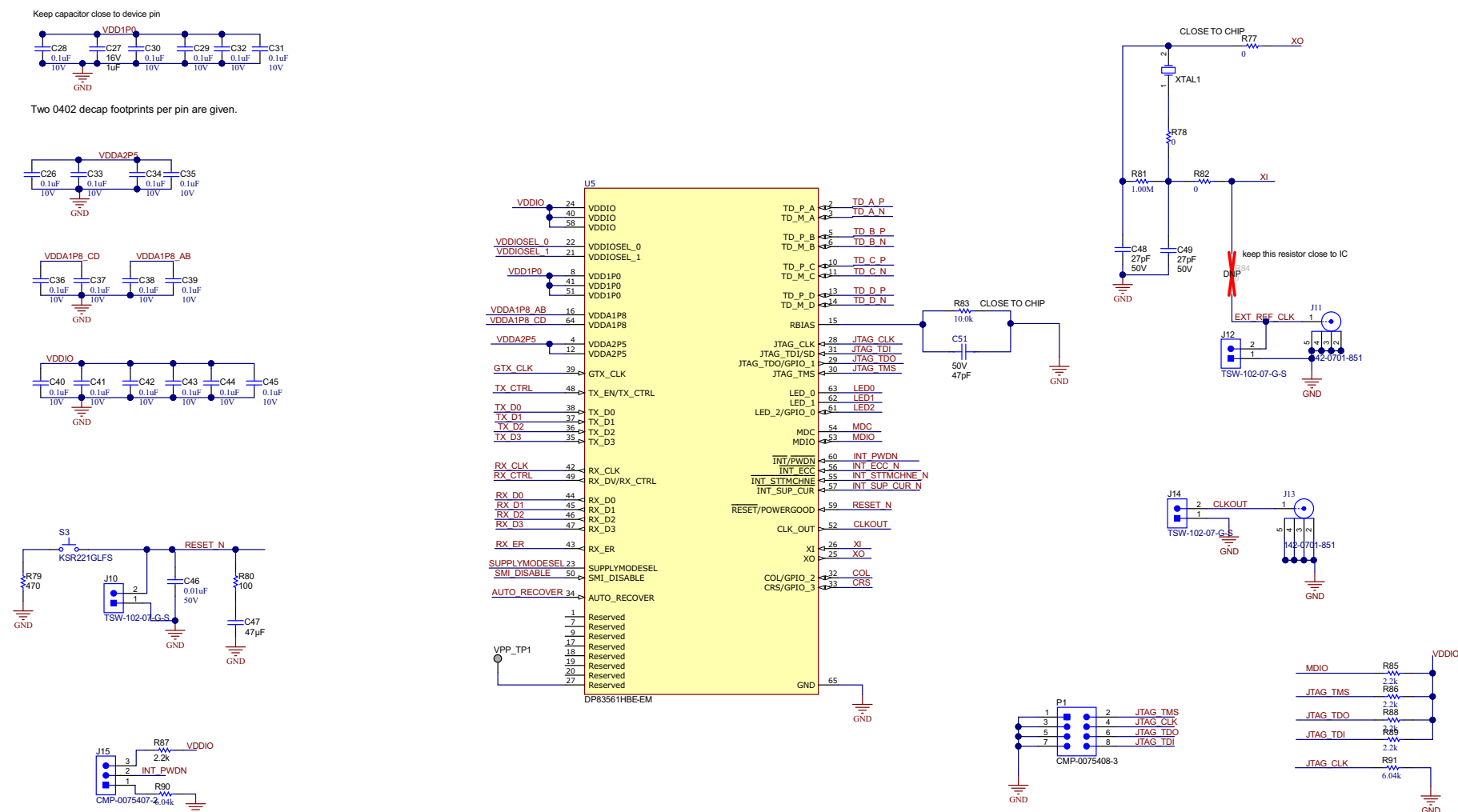


Figure 8-2. DP83561EVM Main Block

8.3 Bootstrap Settings Schematic

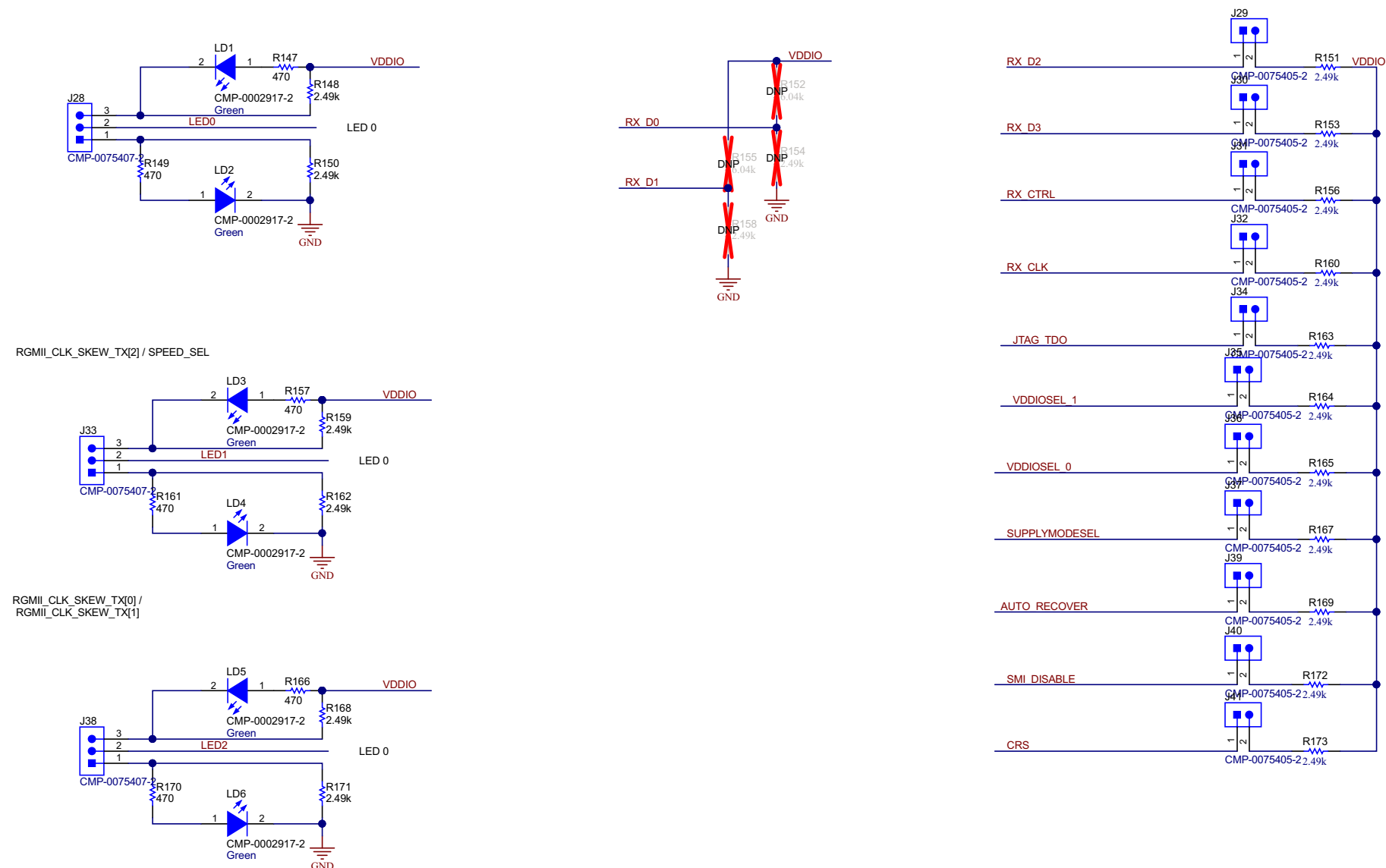


Figure 8-3. DP83561EVM Bootstrap Settings

8.4 Analog Front End and MAC Interface Schematic

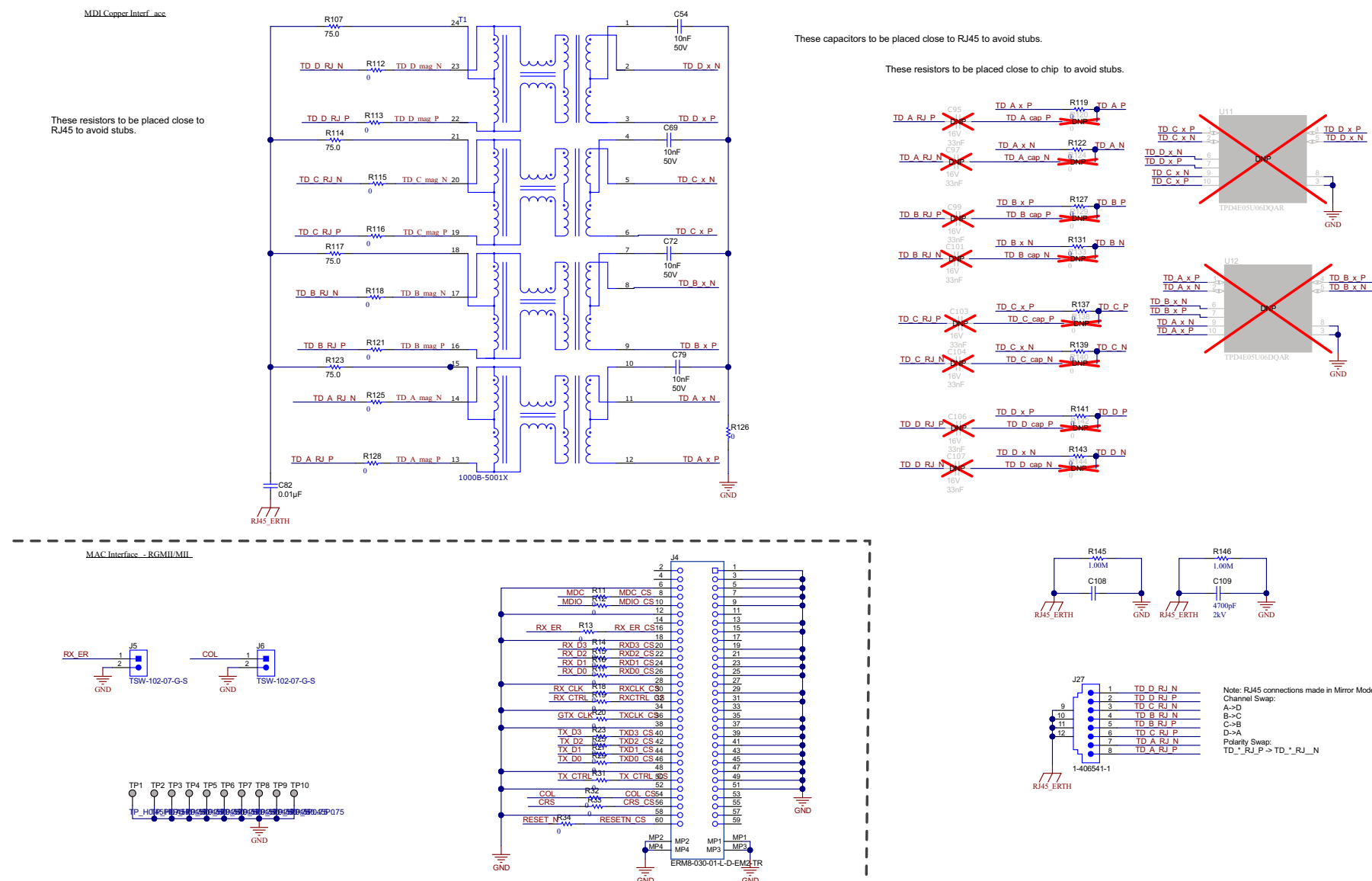


Figure 8-4. DP83561EVM AFE and MAC Interface

8.5 USB Hub Schematic

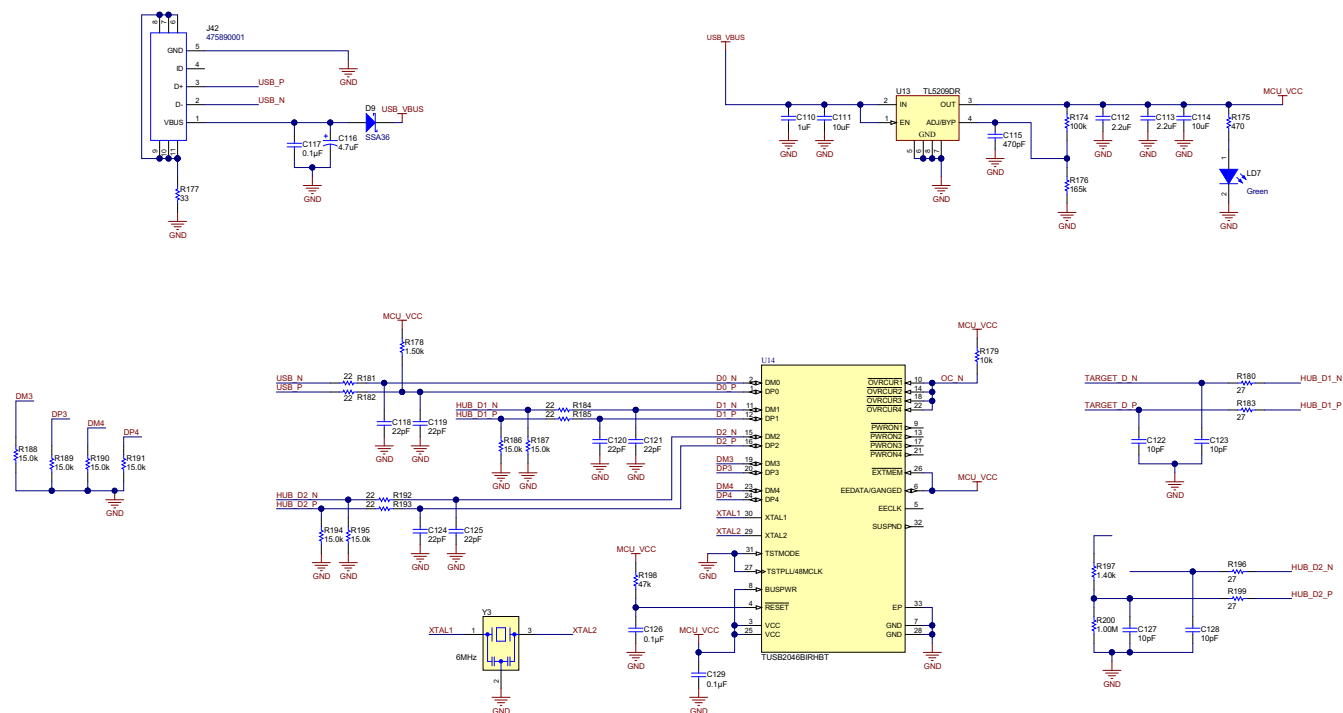


Figure 8-5. DP83561EVM USB Hub

8.6 COMs 1 Schematic

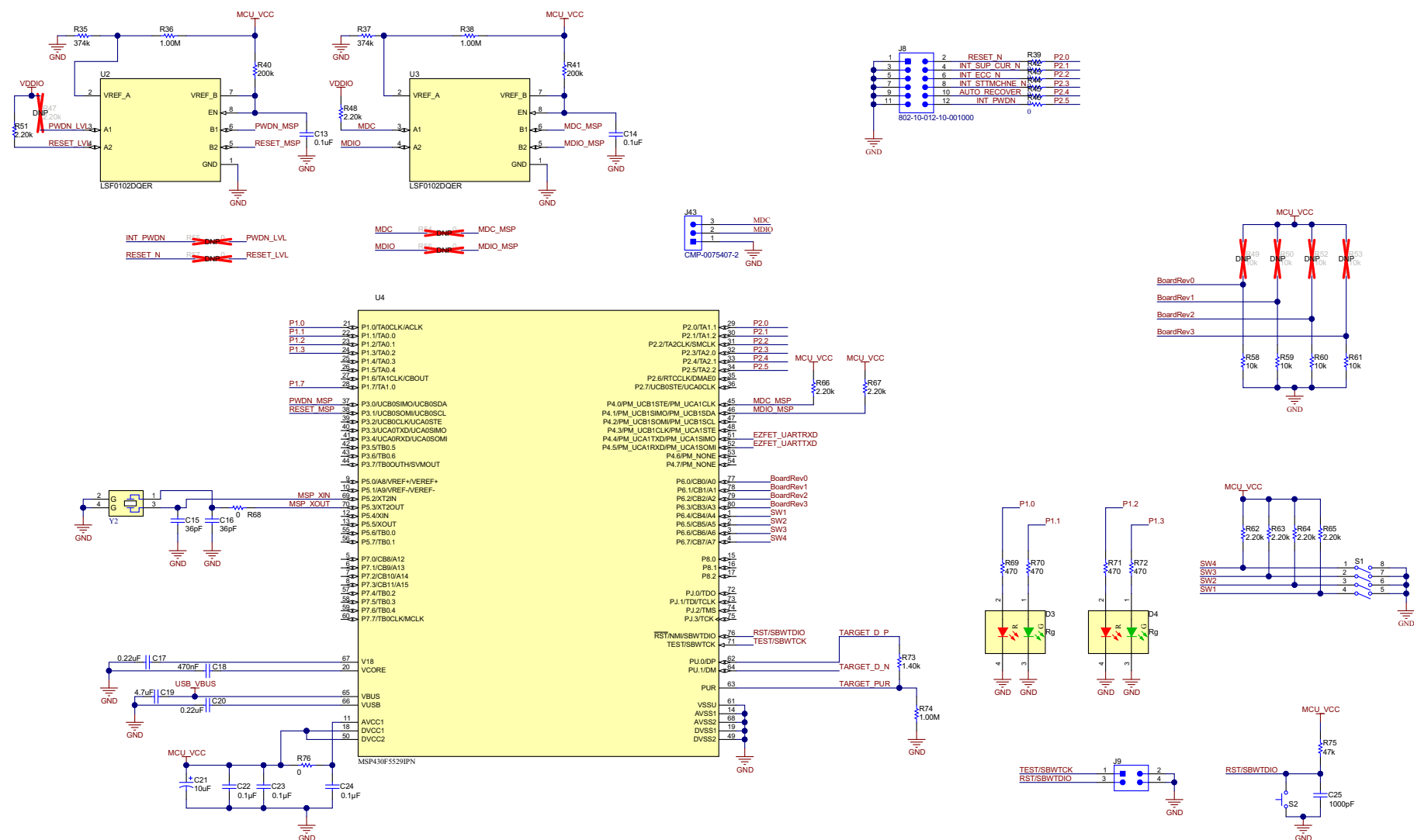


Figure 8-6. DP83561EVM COMs 1

8.8 Breakout Boards Schematic

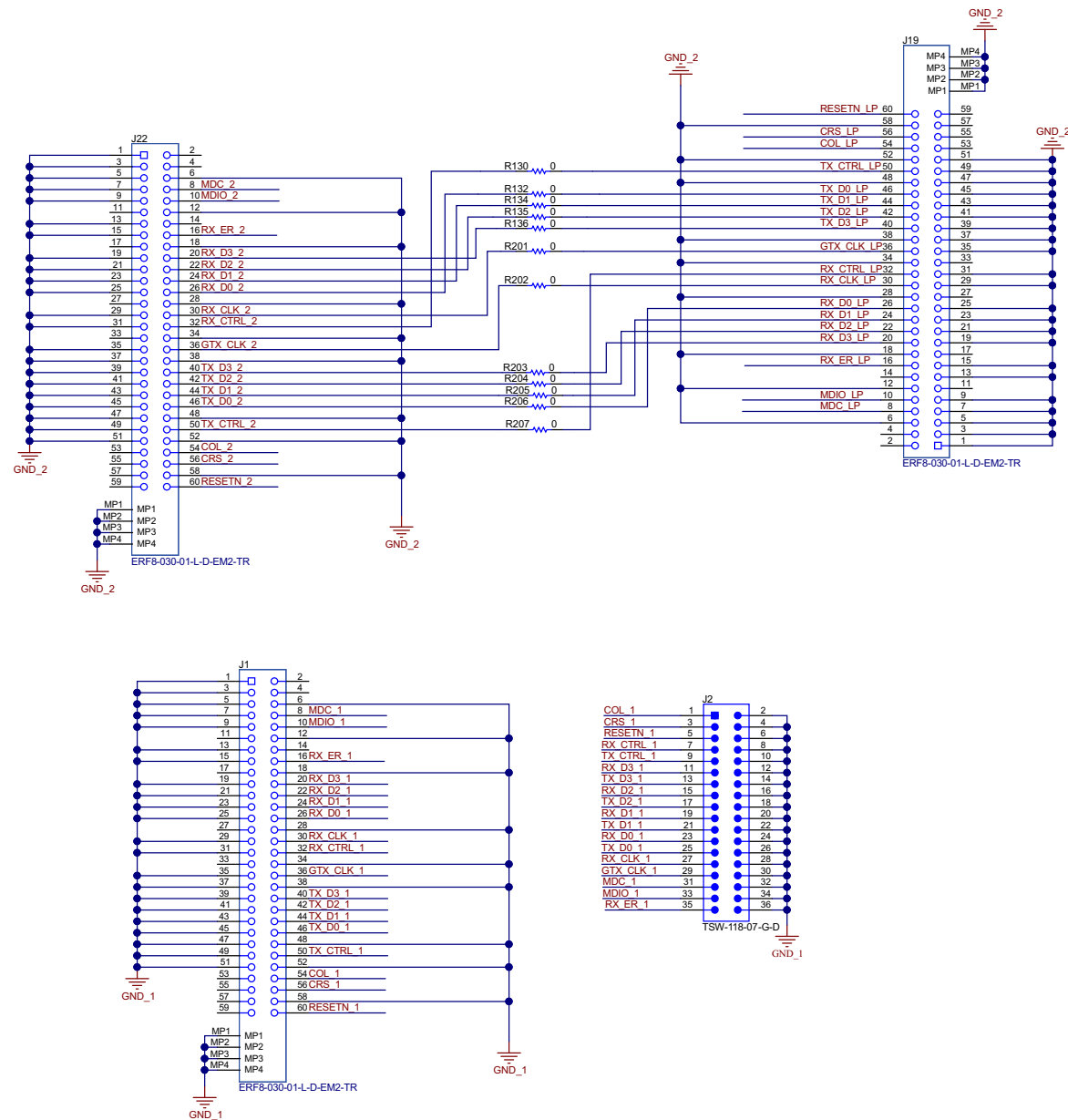
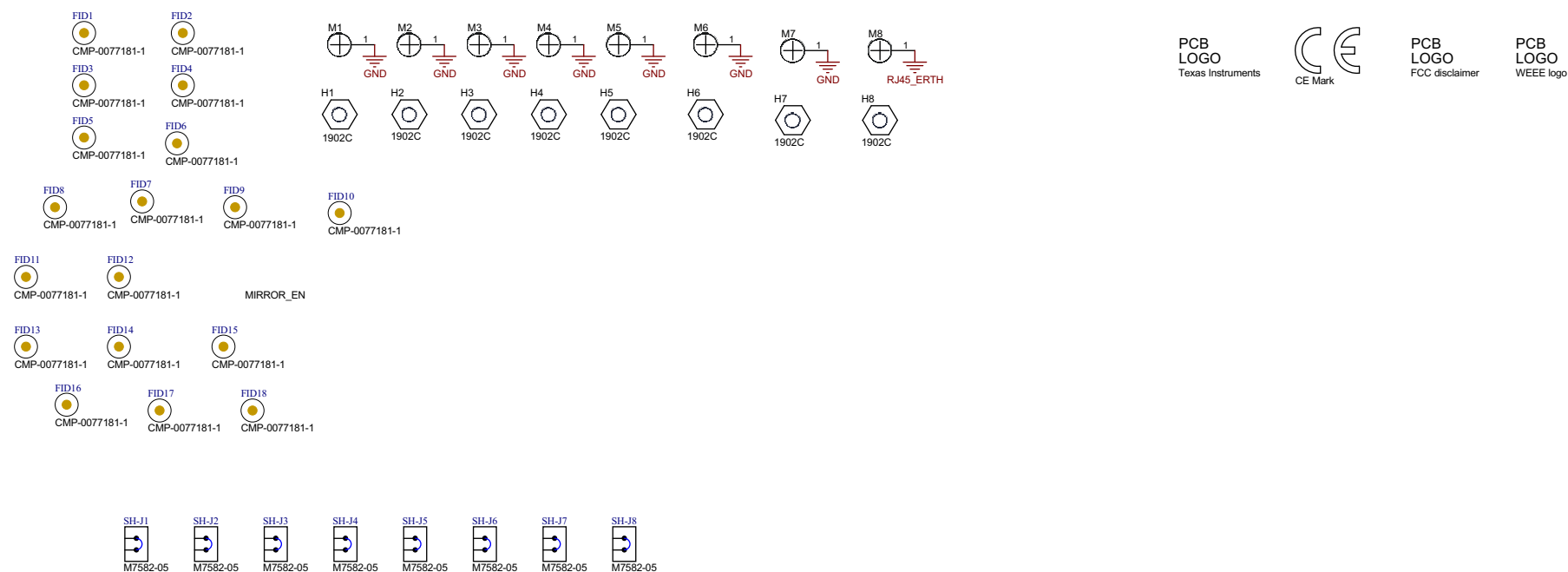


Figure 8-8. DP83561EVM Breakout Connectors

8.9 Hardware Schematic



ZZ1
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ2
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ3
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Figure 8-9. DP83561EVM Hardware

9 Layout

9.1 Top Overlay

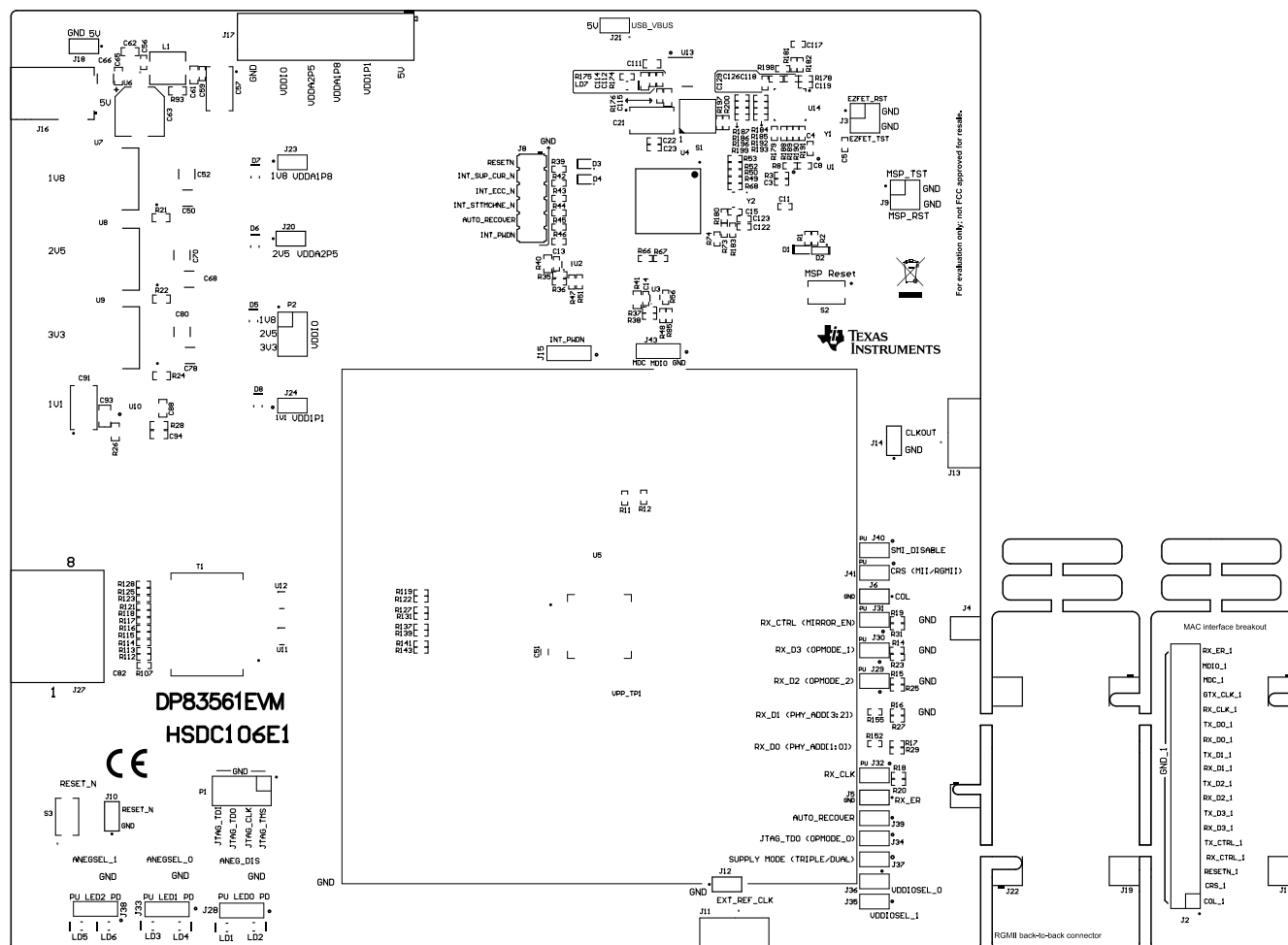


Figure 9-1. Top Overlay

9.2 Top Layer Mask

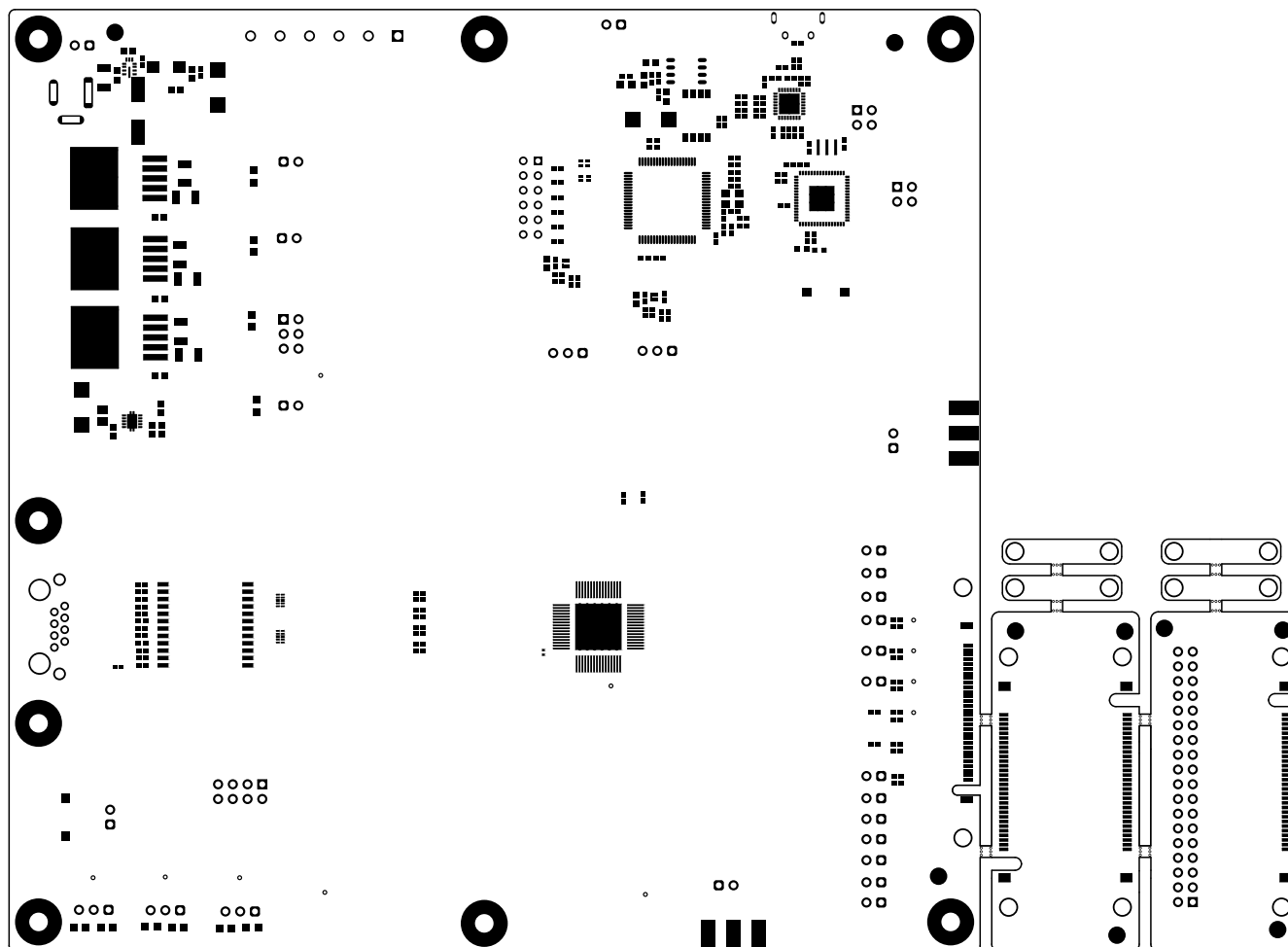


Figure 9-2. Top Layer Mask

9.3 Top Layer

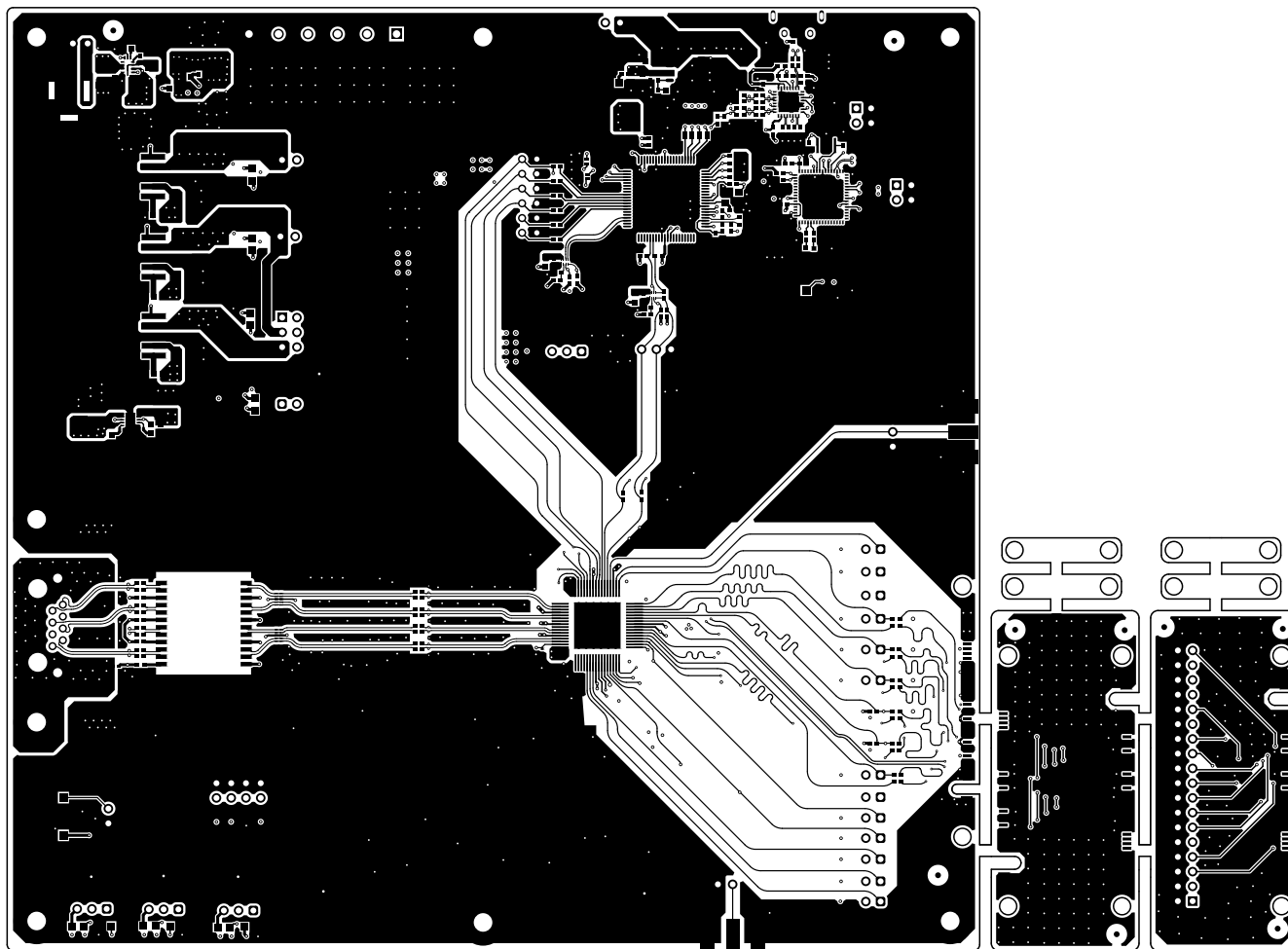


Figure 9-3. Top Layer

9.4 Ground Layer 1

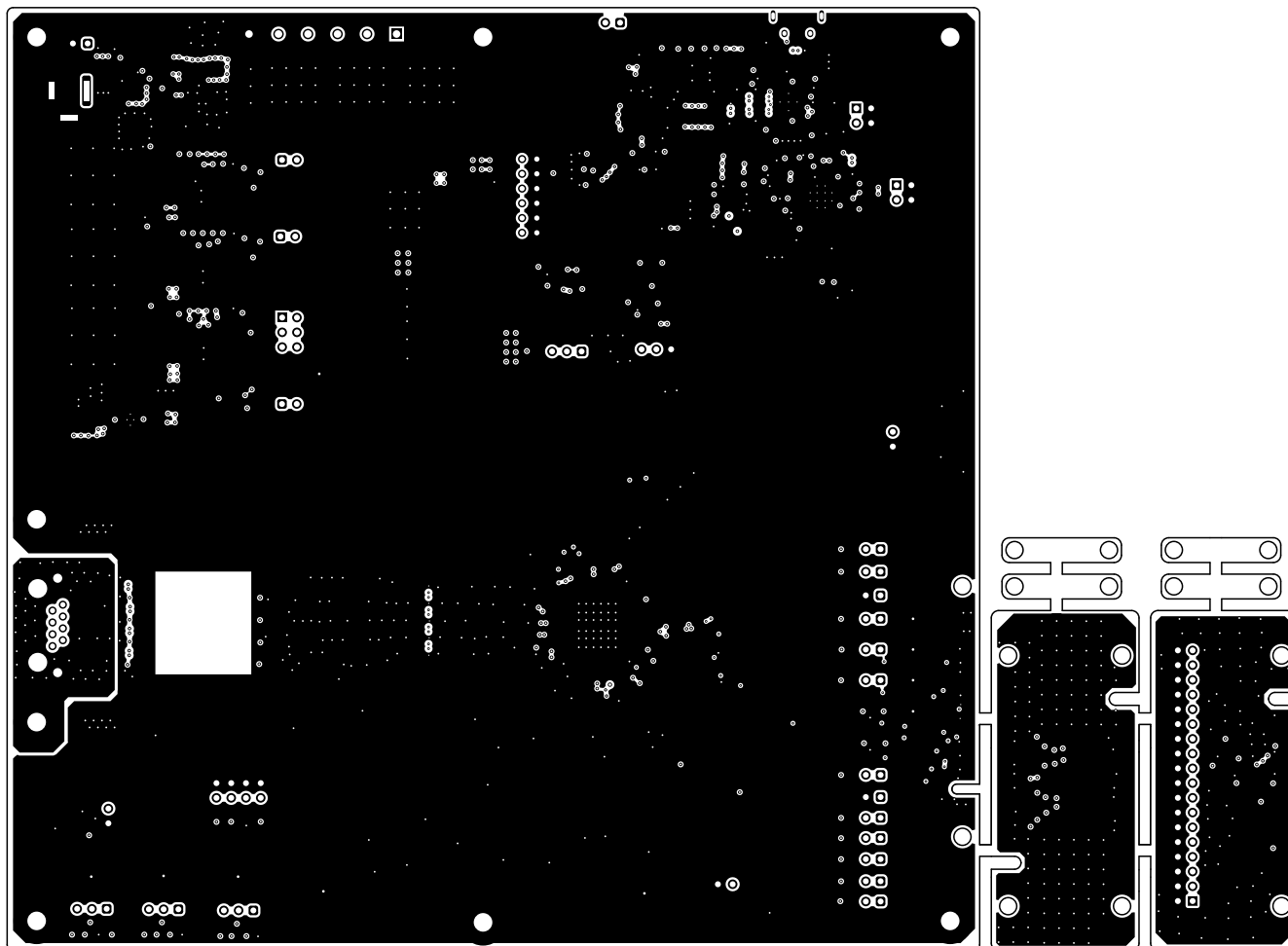


Figure 9-4. Ground Layer 1

9.5 Signal Layer 1

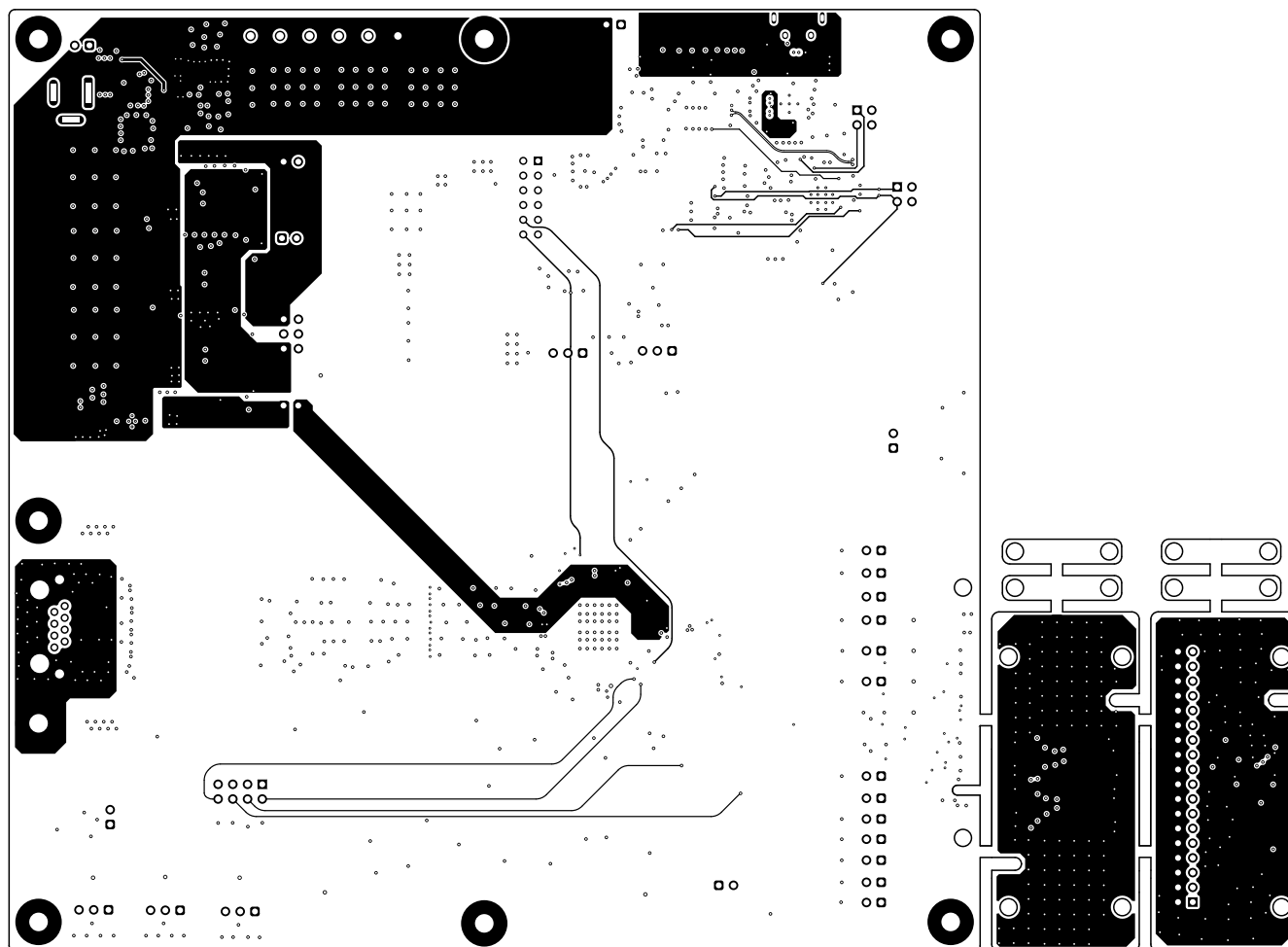


Figure 9-5. Signal Layer 1

9.6 Signal Layer 2

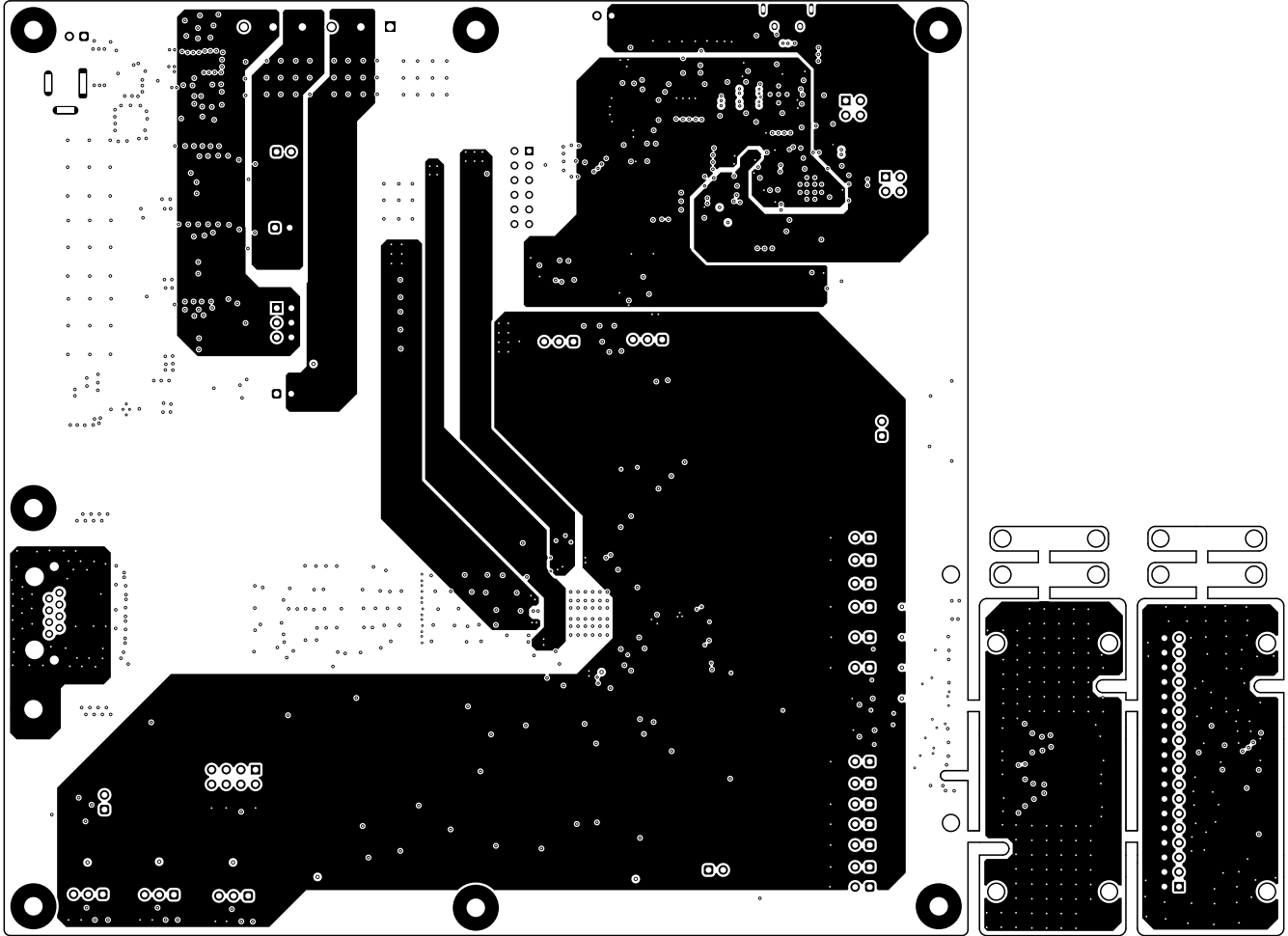


Figure 9-6. Signal Layer 2

9.7 Ground Layer 2

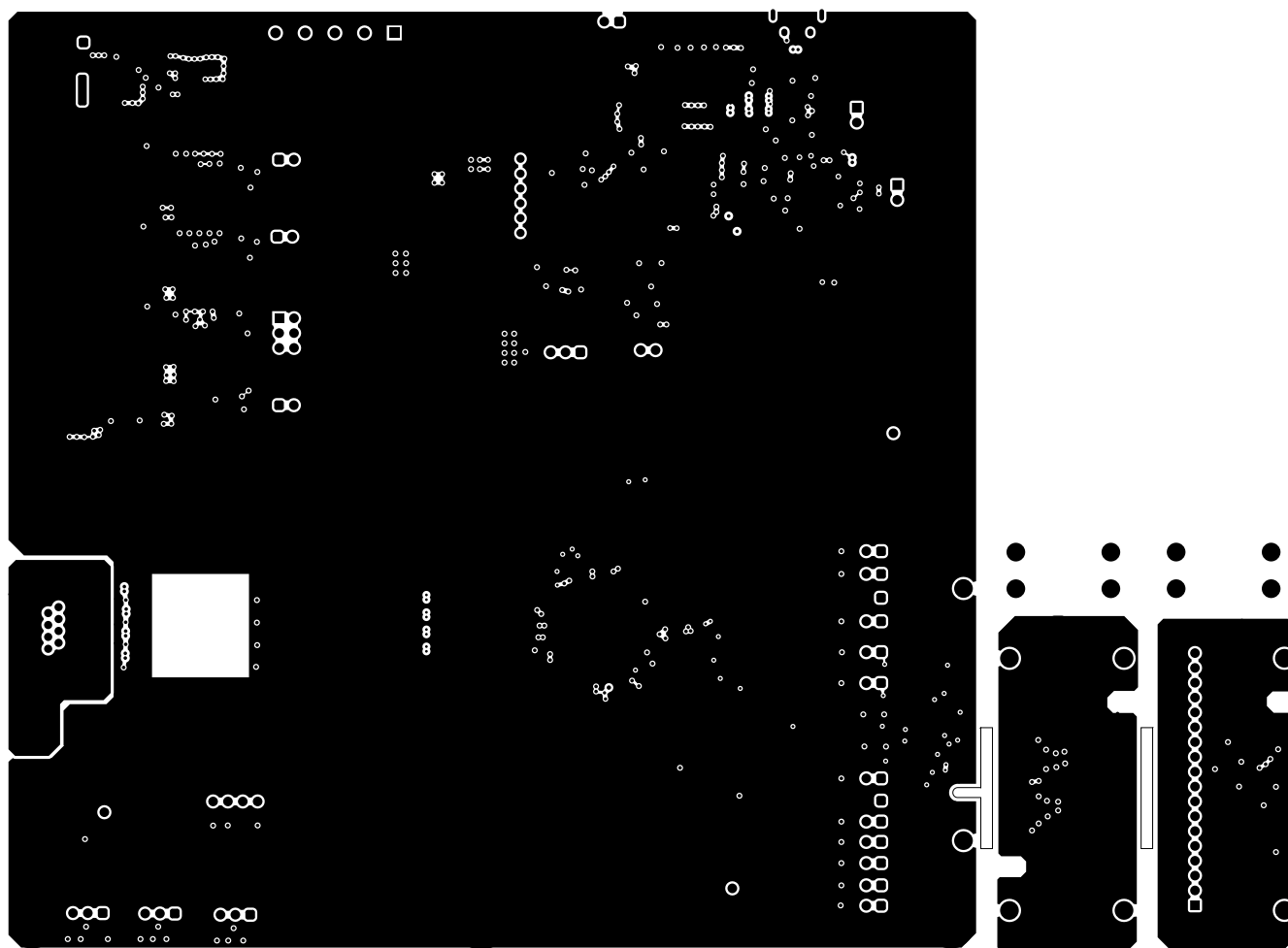


Figure 9-7. Ground Layer 2

9.8 Bottom Layer

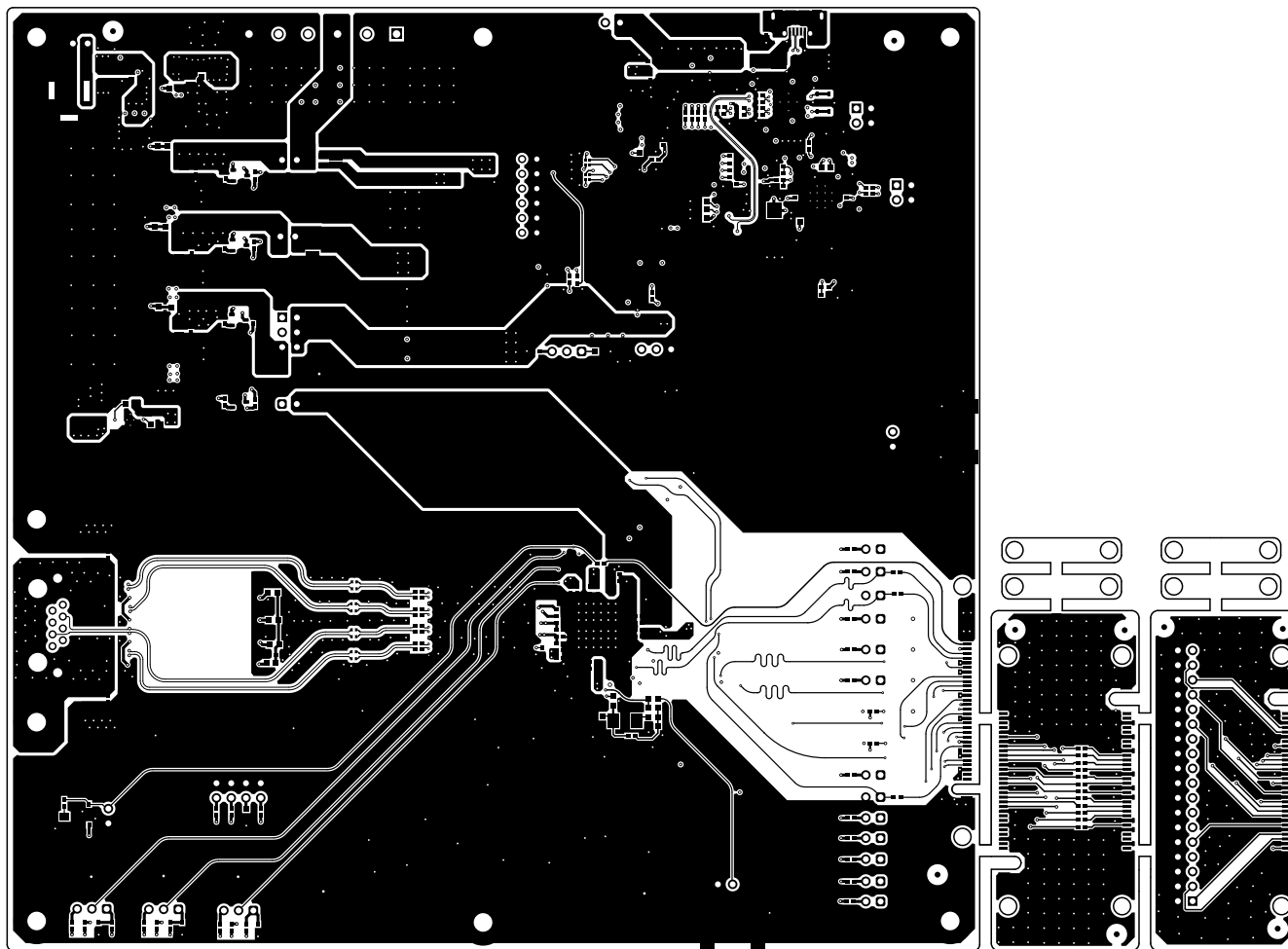


Figure 9-8. Bottom Layer

9.9 Bottom Layer Mask

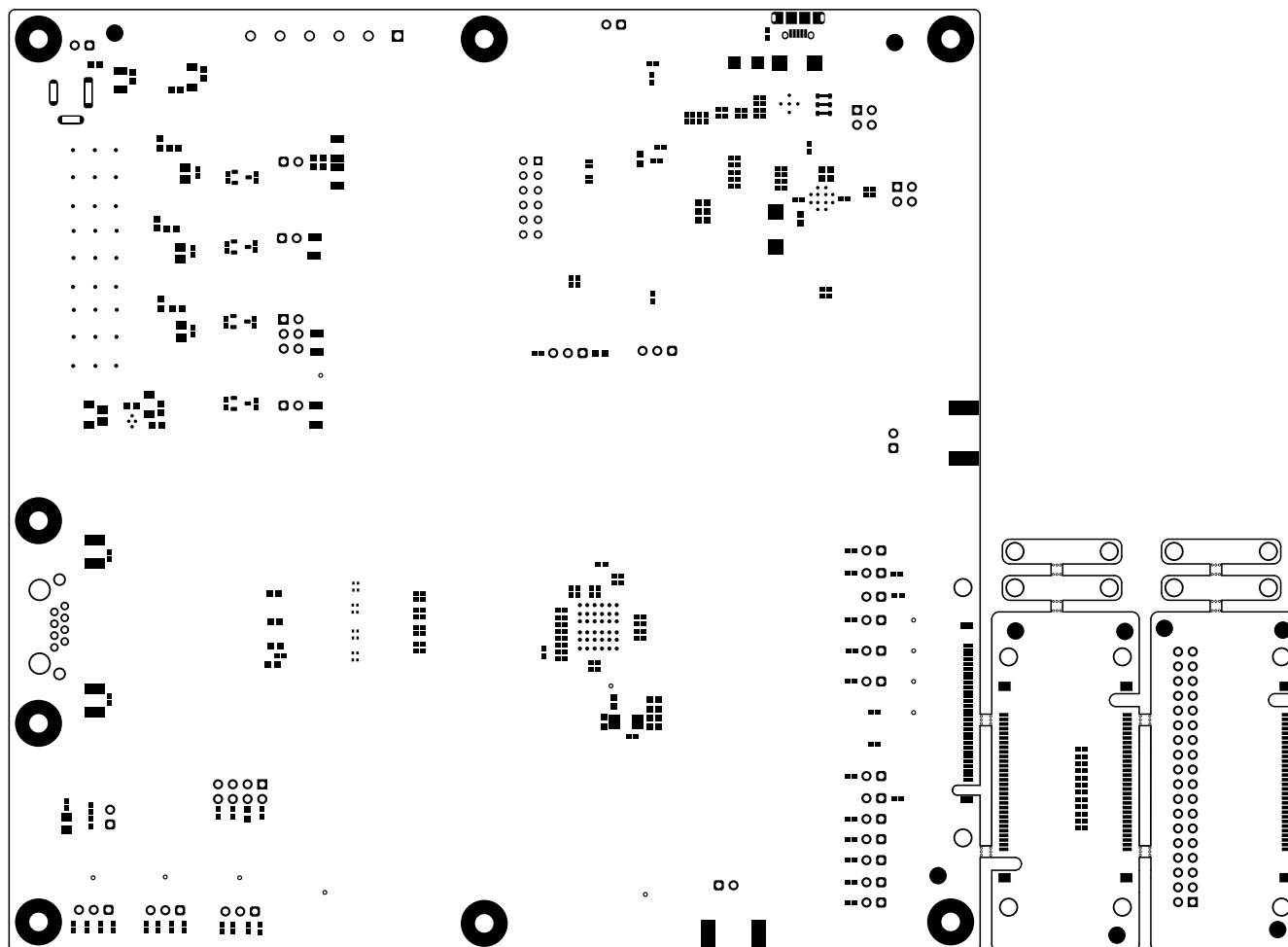


Figure 9-9. Bottom Layer Mask

9.11 Board Assembly

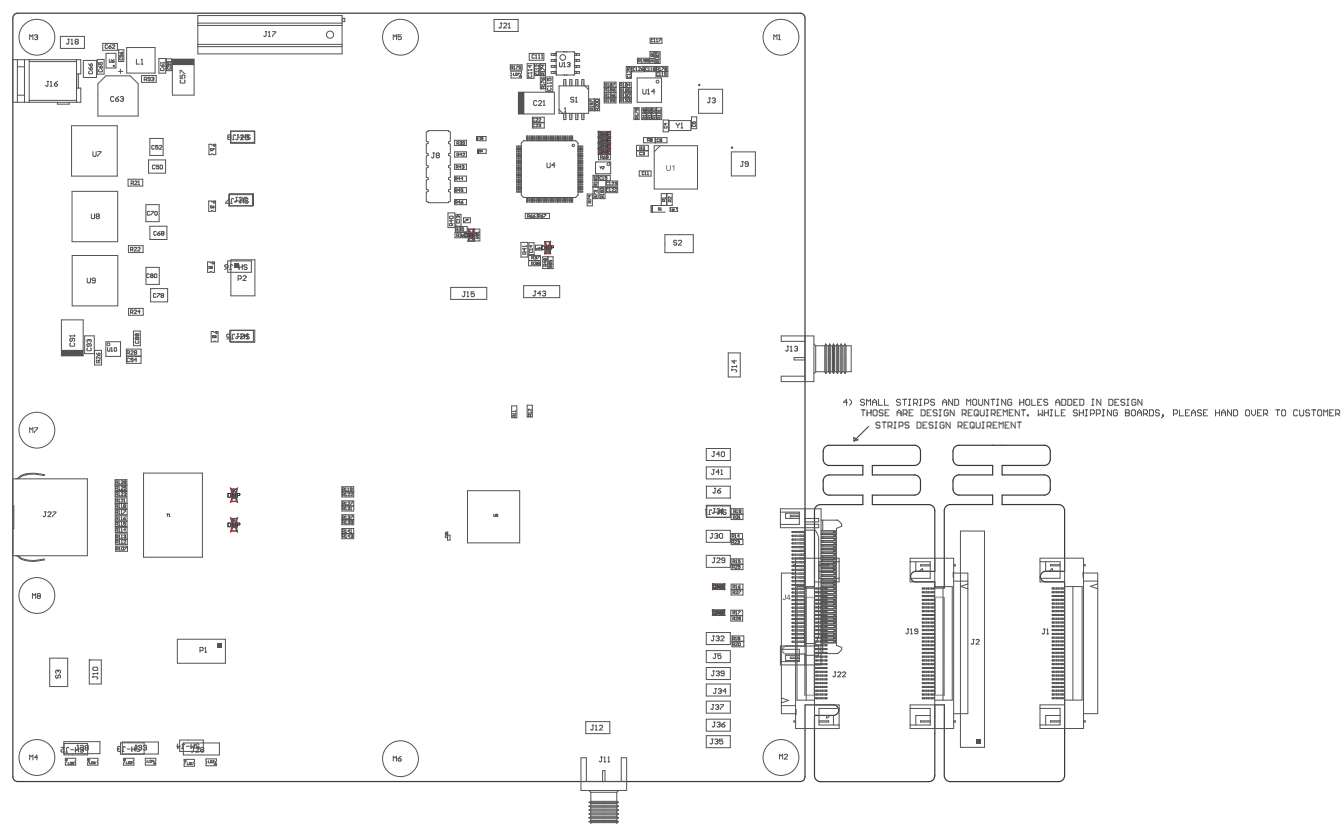
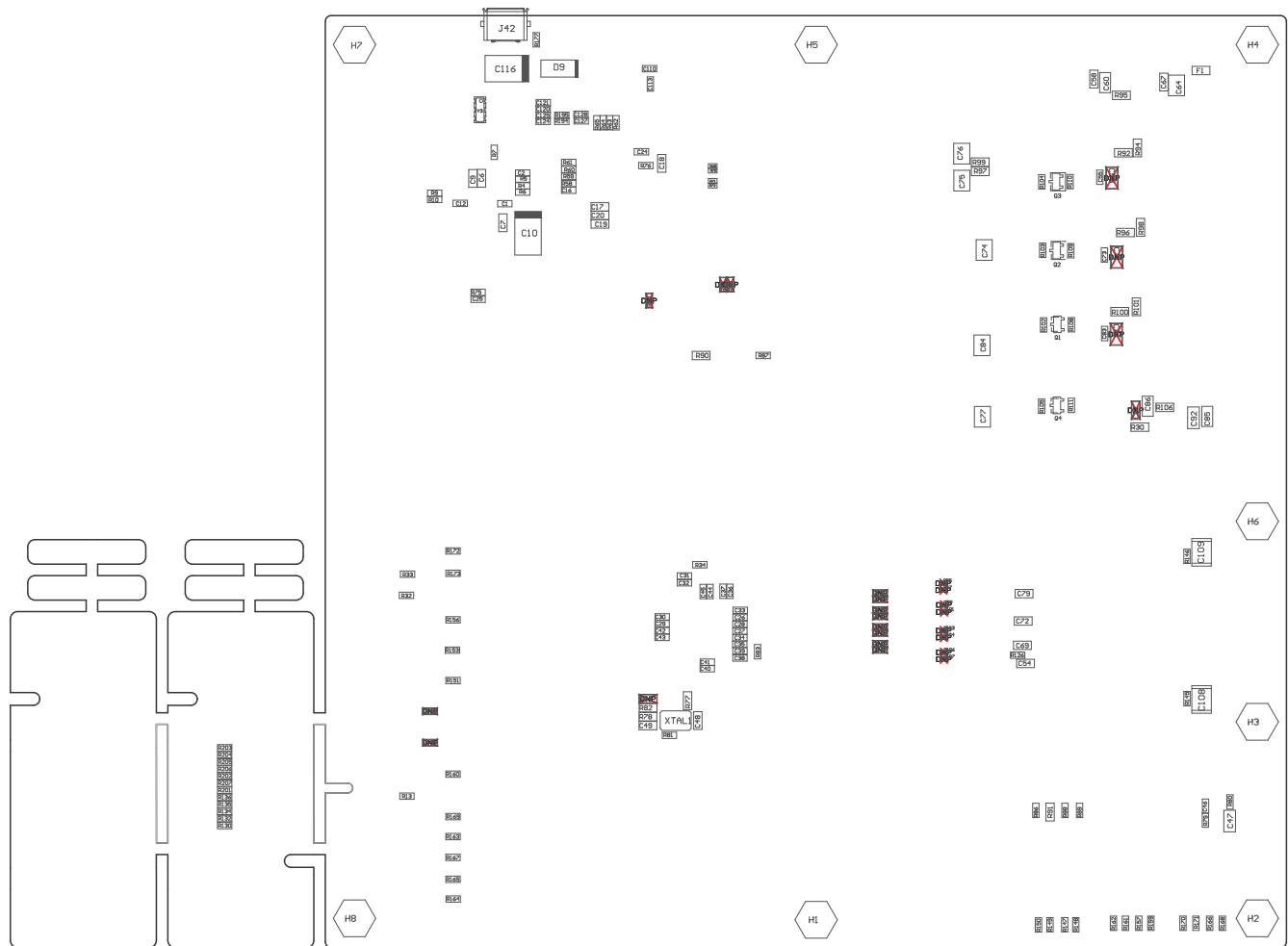


Figure 9-11. Top Assembly



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: 001

Figure 9-12. Bottom Assembly

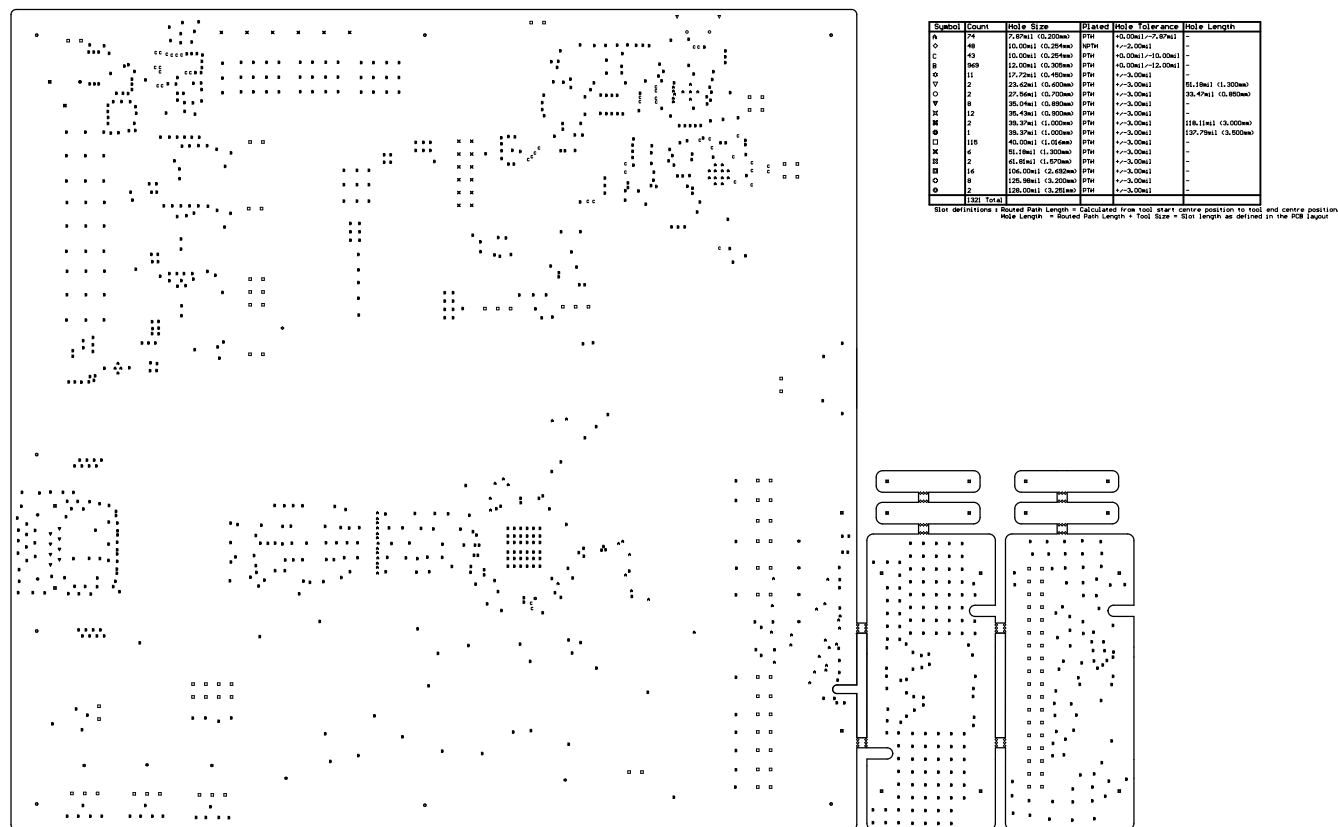


Figure 9-13. Drill Drawing

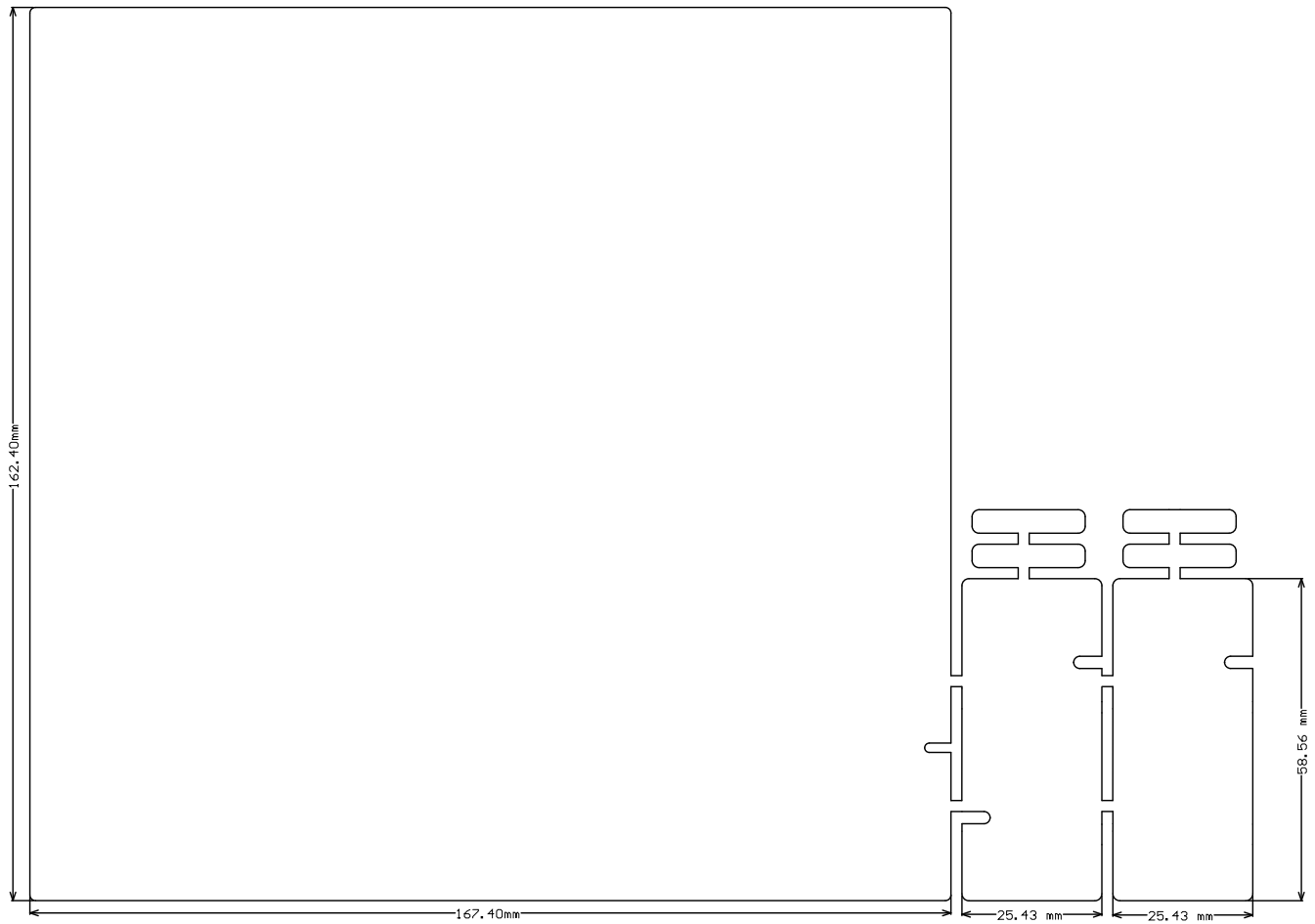


Figure 9-14. Board Dimensions