

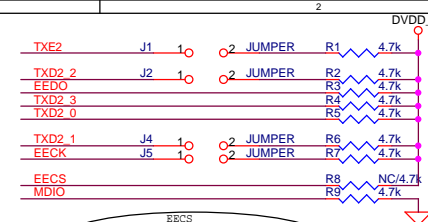
TXE2 (J1)
 0: Port 2 disable
 1: Port 1 disable

TXD2_2 (J2)
 0: Port 2 status form external PHY
 1: Port 2 status in force mode

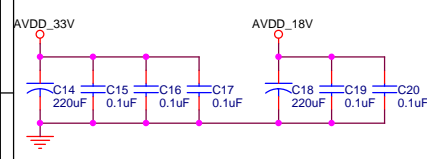
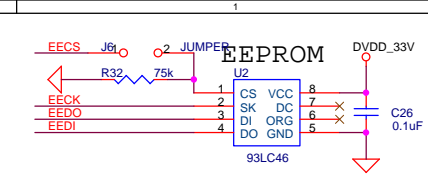
EEDO When Port 2 in force status mode
 0: Port 2 in 100Mbps
 1: Port 2 in 10Mbps

TXD2_3 When Port 2 in force status mode
 0: link on
 1: link off

TXD2_0 When Port 2 in force status mode
 0: Port 2 in full duplex mode
 1: Port 2 in half duplex mode



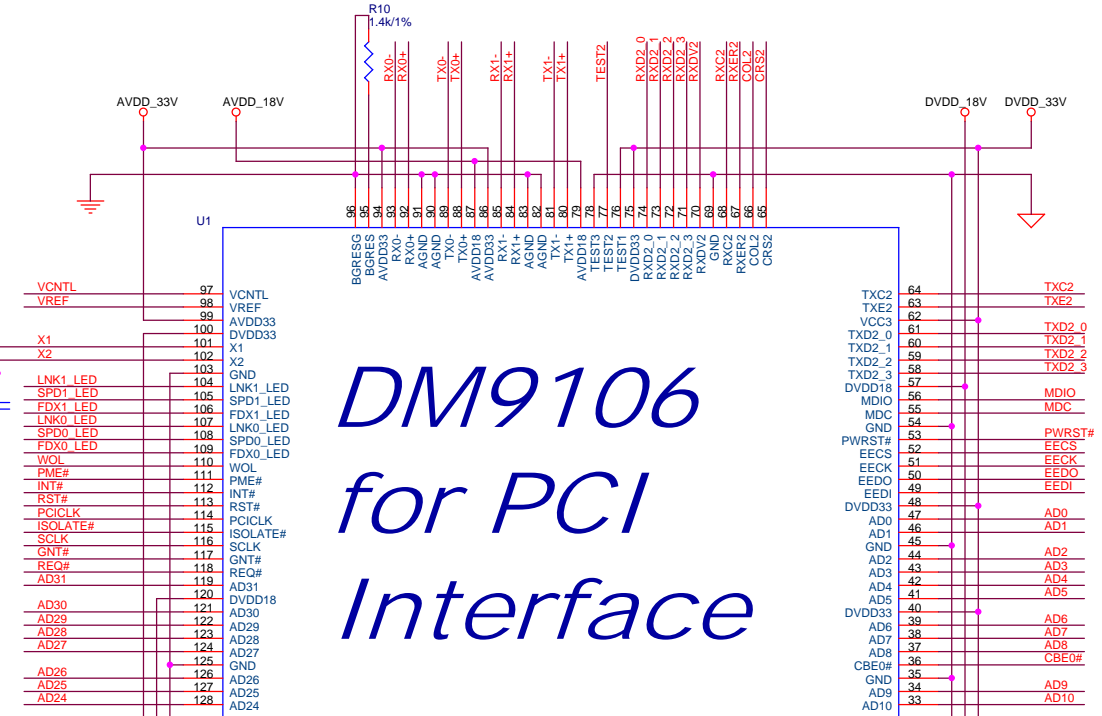
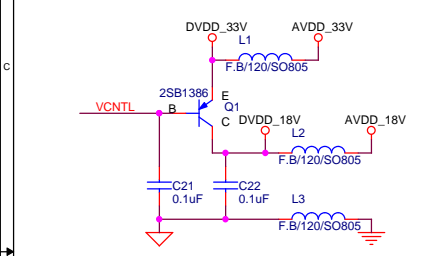
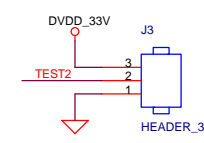
EECS
 Mount R34 use SCLK as system clock
 NC: use internal system clock



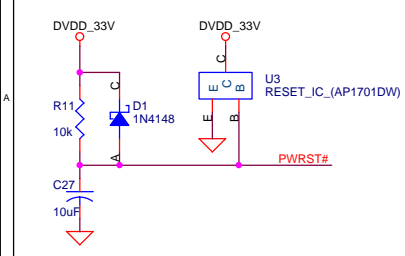
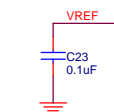
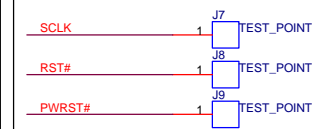
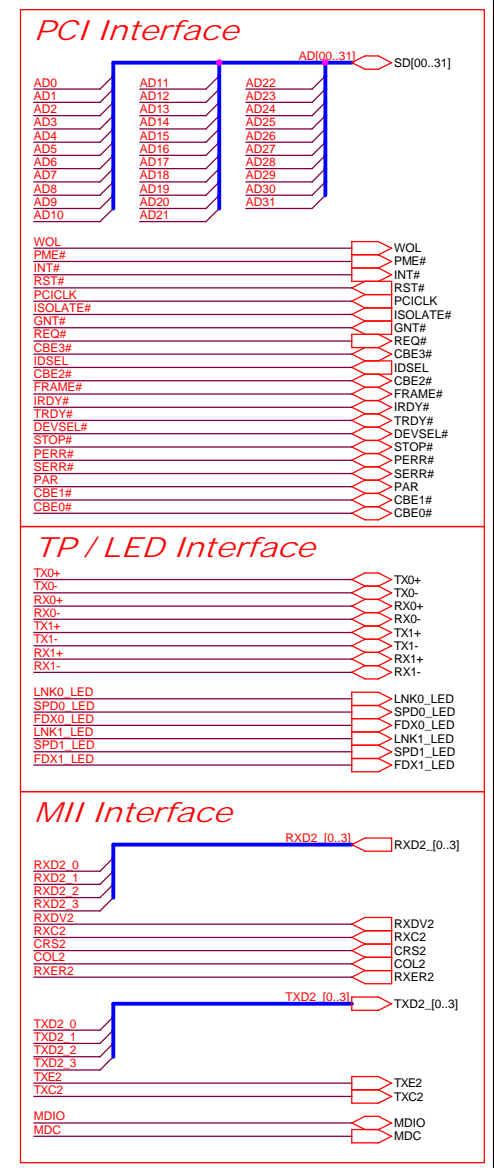
TXD2_1 EECK

0	0	Port 2 is in MII mode (DEFAULT)
0	1	Port 2 is in reverse MII mode
1	0	Port 2 is in RMI mode
1	1	Reserved

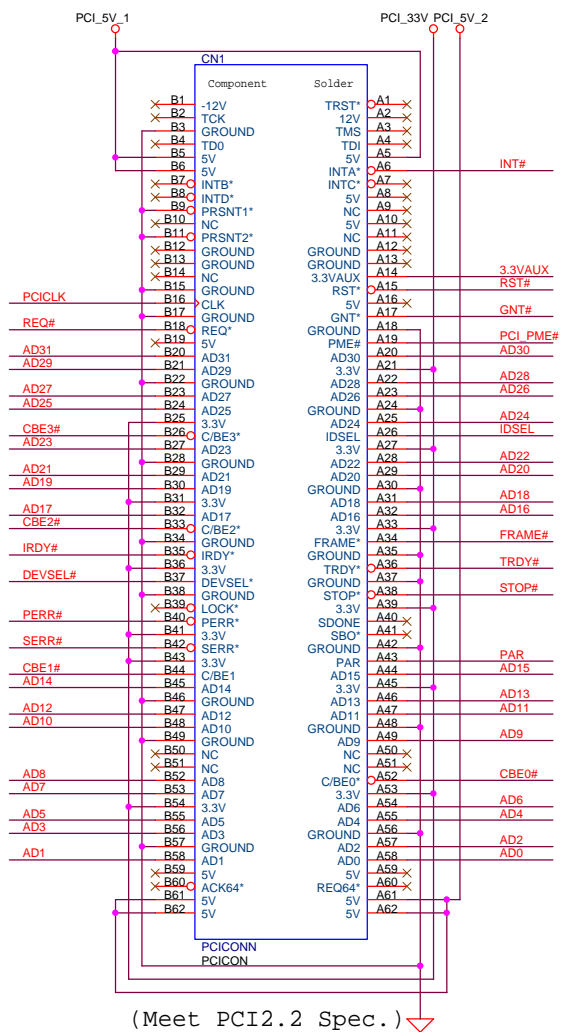
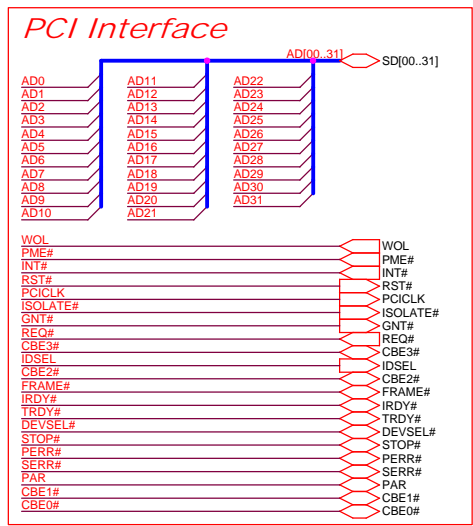
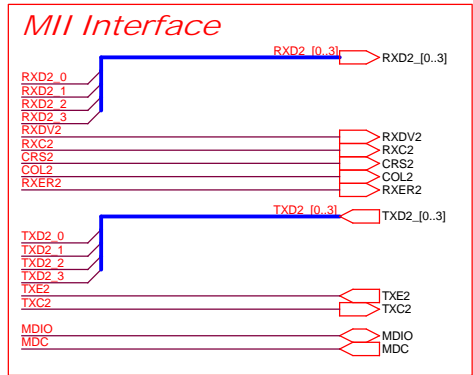
TEST2
 0: 3-Port mode
 1: 2-Port mode
 All ports are active in this mode
 Only 2 ports are active in this mode. Port 1 or Port 2 can be disabled by strap TXEN2. In this mode, the memory resource is shared by PCI bus port and the other port



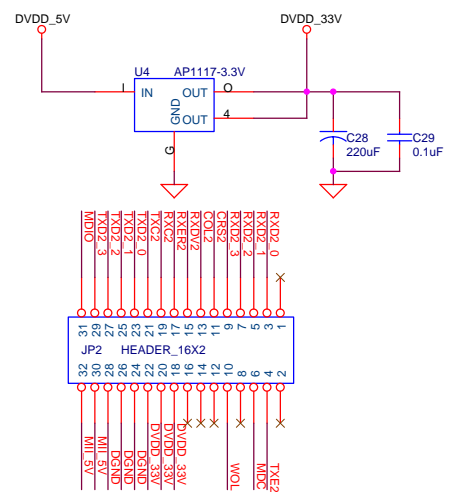
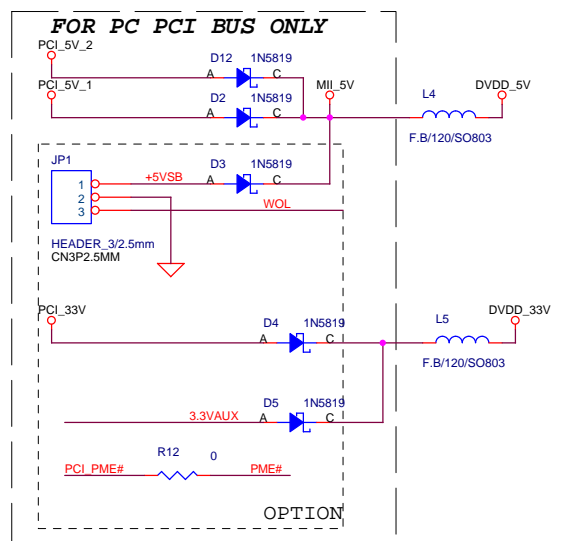
DM9106 for PCI Interface



Davicom Semiconductor Inc.		
Title		
3 Port Switch + PCI Interface Chip		
Size	Document Number	Rev
A3	DM9106_EVB_BOARD	1.0
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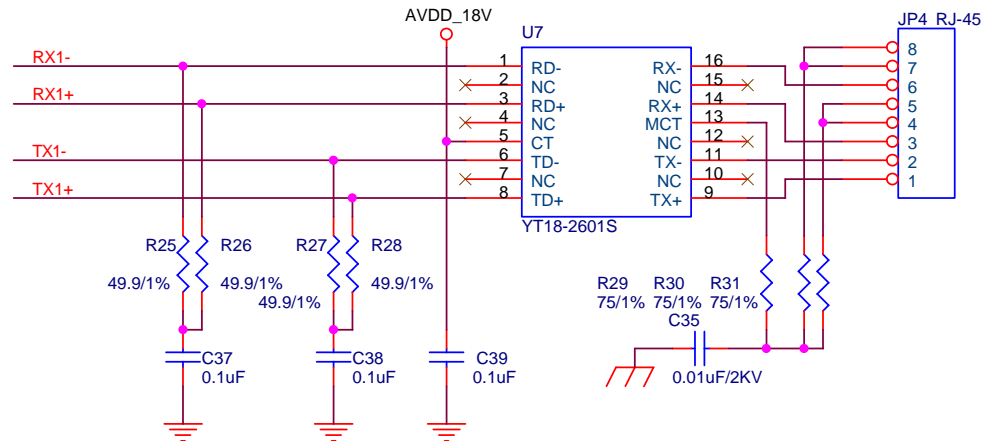
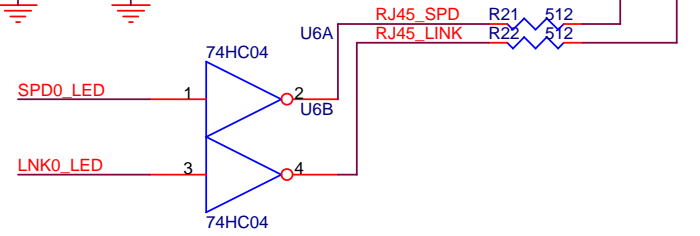
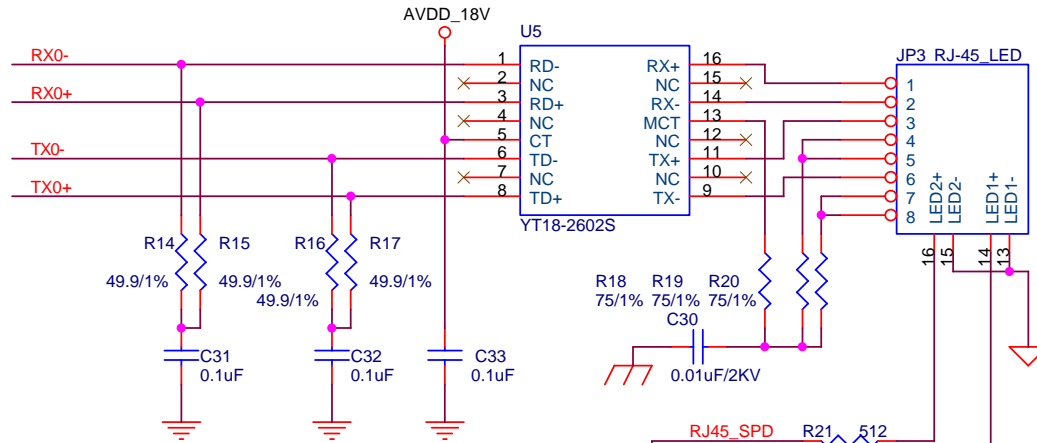
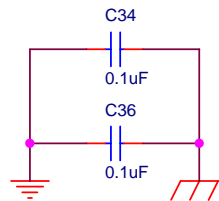
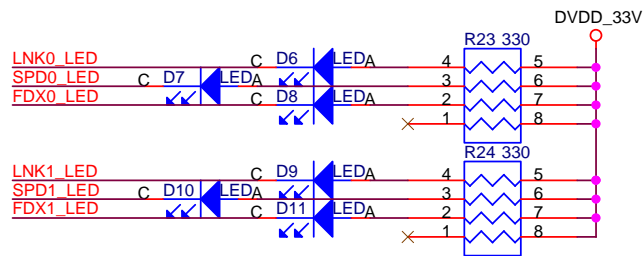


(Meet PCI2.2 Spec.)



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TP / LED Interface



Davicom Semiconductor Inc.		
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