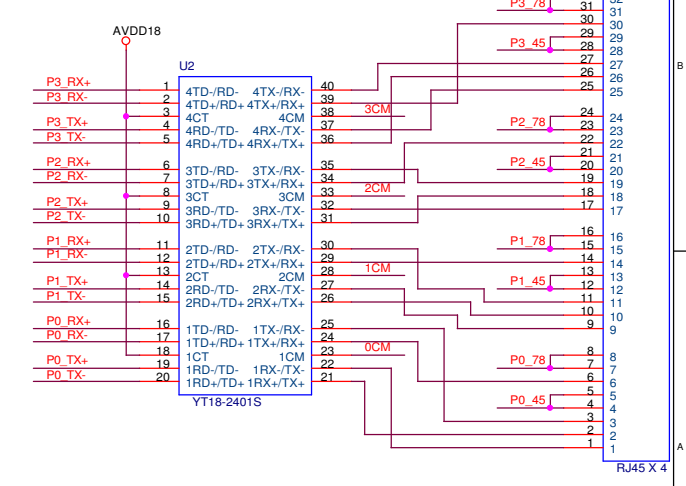
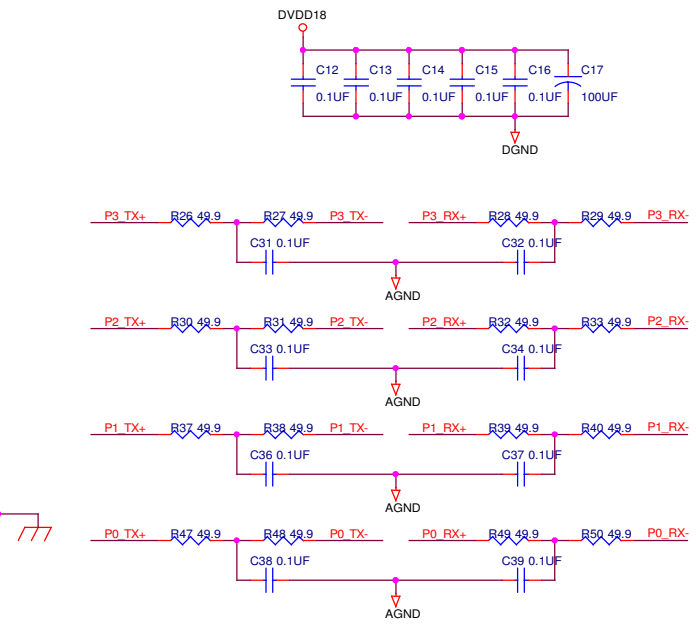
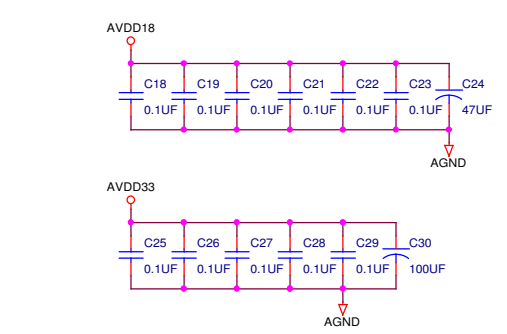
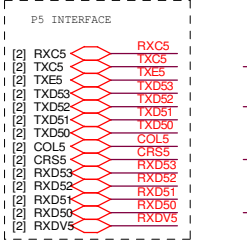
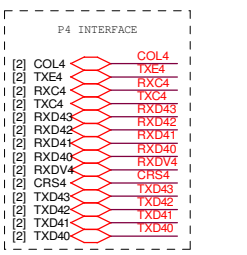
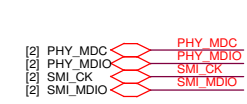
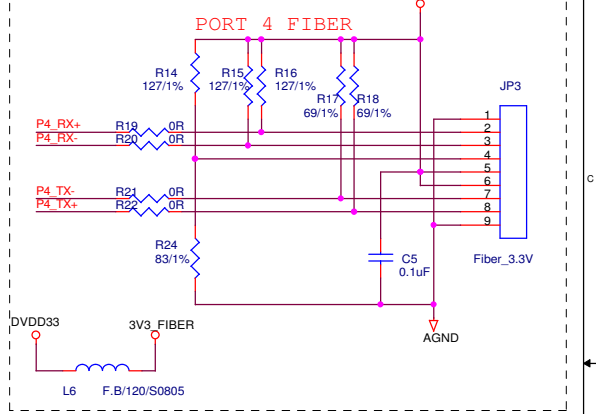
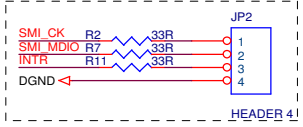
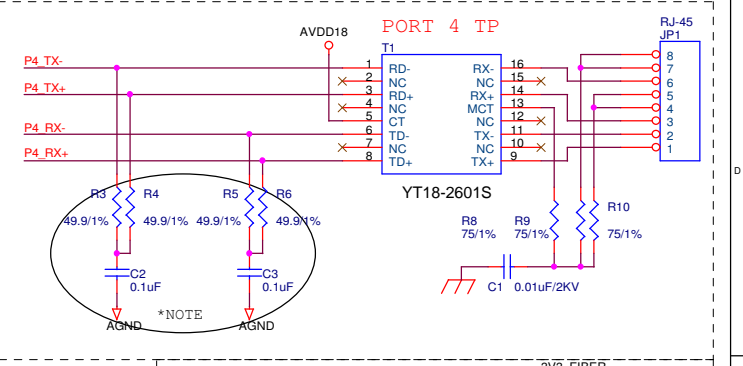


Choose TP or Fiber to use
WHEN USE FIBER MODULE, MUST CHANGE IC PART OF THE TP COMPONENT

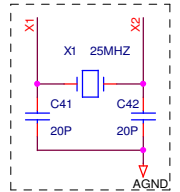
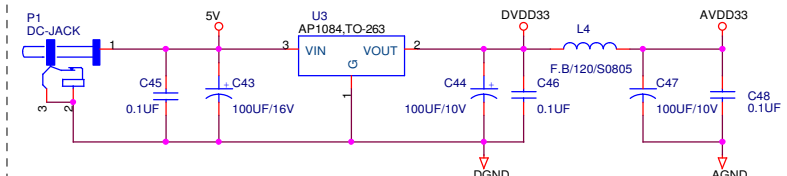
R3	182R/1%
R4	182R/1%
R5	83R/1%
R6	83R/1%
C2	0R
C3	0R

*NOTE

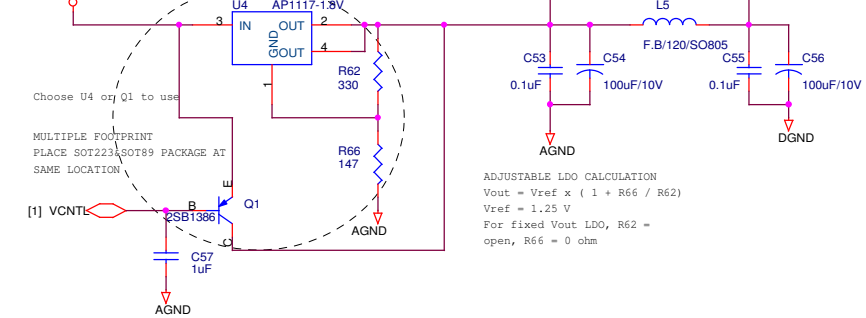


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Title	DM8806 DEMO BOARD		
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A3	SWITCHE6_MAIN		
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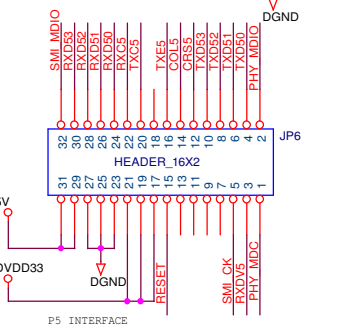
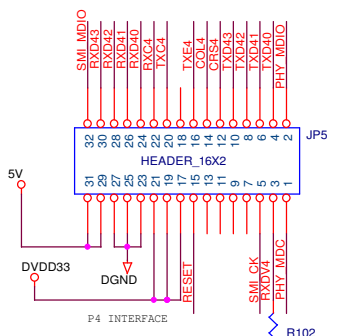
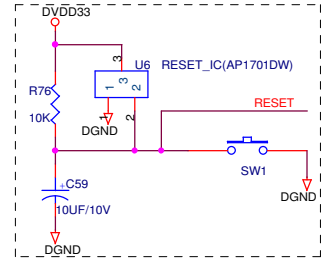
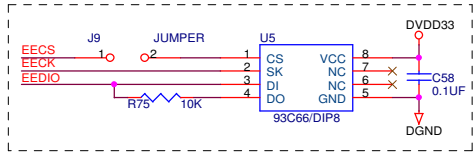
Power 5V TO 3.3V



Power 3.3V TO 1.8V

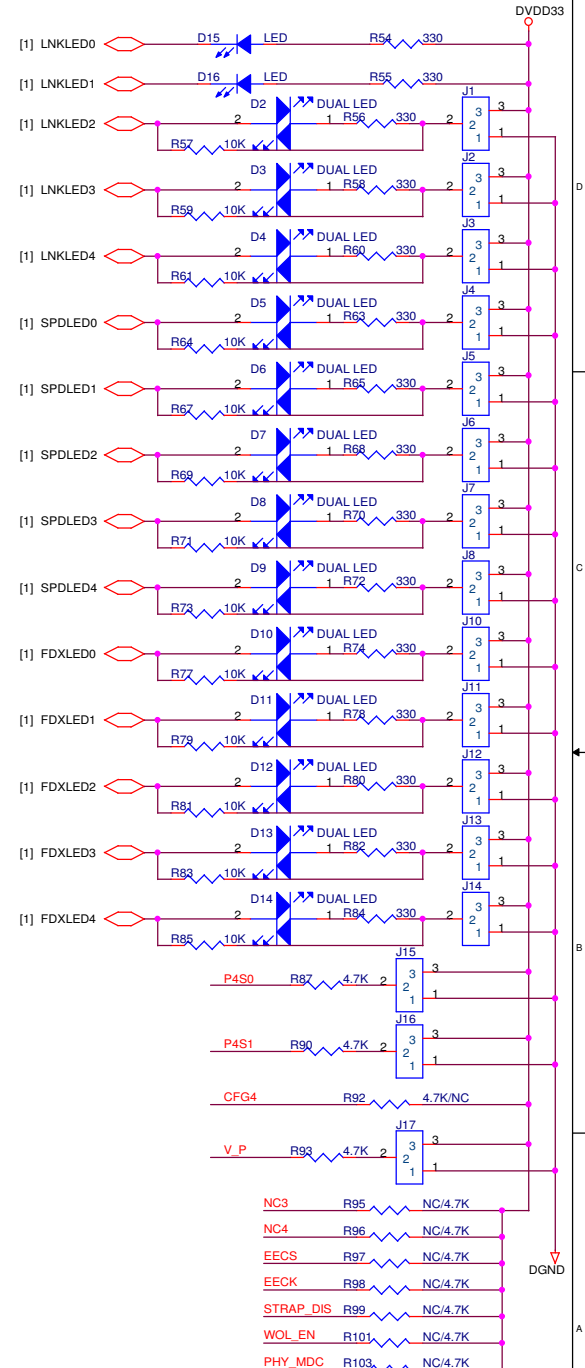


- [1] SMI_CK SMI_CK
- [1] SMI_MDIO SMI_MDIO
- [1] NC3 NC3
- [1] NC4 NC4
- [1] PHY_MDIO PHY_MDIO
- [1] PHY_MDC PHY_MDC
- [1] EECS EECS
- [1] EECK EECK
- [1] EEDIO EEDIO
- [1] X1 X1
- [1] X2 X2
- [1] RESET RESET
- [1] P4S0 P4S0
- [1] P4S1 P4S1
- [1] P4S4 P4S4
- [1] CFG4 CFG4
- [1] STRAP_DIS STRAP_DIS
- [1] WOL_EN WOL_EN



MII	RMII	RevMII	EXTERNAL MII
TXC		TXC	RXC
TXE	TXE		TXC
TXD3		TXE	RXDV
TXD2		TXD3	RXD3
TXD1	TXD1	TXD2	RXD2
TXD0	TXD0	TXD1	RXD1
RXDV	RXDV	TXD0	RXD0
RXC	RXC	RXDV	TXE
RXD3		RXD3	TXD3
RXD2		RXD2	TXD2
RXD1	RXD1	RXD1	TXD1
RXD0	RXD0	RXD0	TXD0
COL		COL	CRS
CRS	CRS_DV		COL
MDC			RXER
MDIO	MDIO		

WOL_EN	Wake On LAN Enable	0: disable 1: Enable to detect WOL magic packet event	
PHY_MDC	PORT 0 AND 1 TRUNK PORTS ENABLE	0: Disable 1: Enable	
LNKLED1	802.3az Energy Efficient Ethernet function for all ports	0: Disable 1: Enable	
LNKLED3,2	J2 J1 Default: 1 1	Reserved	
LNKLED4	Port 4 PHY TP mode in M3A or M3C mode	1: Copper mode 0: fiber mode	
SPDLED0	When in M3B, Port4 in force mode	0: Half-duplex mode 1: Full-duplex mode	
SPDLED1	When in M3B, Port4 in force mode	0: 10M mode 1: 100M mode	
SPDLED3,2	Port 4 in M3B Mode	0 0 RevMII with TXC4 turbo clock 0 1 RMII 1 0 MII 1 1 RevMII with TXC4 25MHz/2.5MHz clock	
SPDLED3	SPDLED2	Port 4 in M3C Mode	0 X Reserved, do not use 1 X PHY_MII
SPDLED4	When in M3B / M3C and Port4 in force mode	0: link OFF 1: link ON	
FDXLED0	When Port5 in force mode	0: 10M mode 1: 100M mode	
FDXLED1	When Port5 in force mode	0: 10M mode 1: 100M mode	
FDXLED3,2	Port 5 Mode	0 0 Reserved, do not use 0 1 RMII 1 0 MII 1 1 RevMII	
FDXLED3	FDXLED2	When Port5 in force mode	0: link OFF 1: link ON
FDXLED4	When Port5 in force mode	0: link OFF 1: link ON	
STRAP_DIS	Strap pins disabled	0: strap pins enabled 1: no strap pin function	
SP100(NC3)	Flow Control in PHY Register 4 bit 10	0: bit value is "1" 1: bit value is "0"	
SP101(NC4)	Default: 0	Reserved	
EECS	Port 5 link/duplex/speed mode in MII/RMII	0: force mode 1: PHY_MDC/PHY_MDIO polling mode	
EECK	When in M3B , Port 4 link/duplex/speed mode in MII/RMII	0: force mode 1: PHY_MDC/PHY_MDIO polling mode	
Port 4 operation mode			
CFG4	P4_SET1[16] P4_SET0[15]	0 0 0 use internal PHY(M3A) 0 0 1 MII/RMII/RevMII(M3B) 1 X X TP MII (M3C)	
V_P J17	Default: 0	Reserved	



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VER	DATE	ENGINEER	NOTE
1.0	11/16/2010	MARCO FAN	NEW CIRCUIT
2.0	01/31/2011	MARCO FAN	Modify: 1. RXD0 Connect 4.7K to DGND 2. Dual LED add 10K fix Dual LED bug 3. IC pin define error , pin98 & pin100 Exchange
2.0	03/01/2013	WILLIE NIOU	RENAME FOR DM8806 CIRCUIT

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