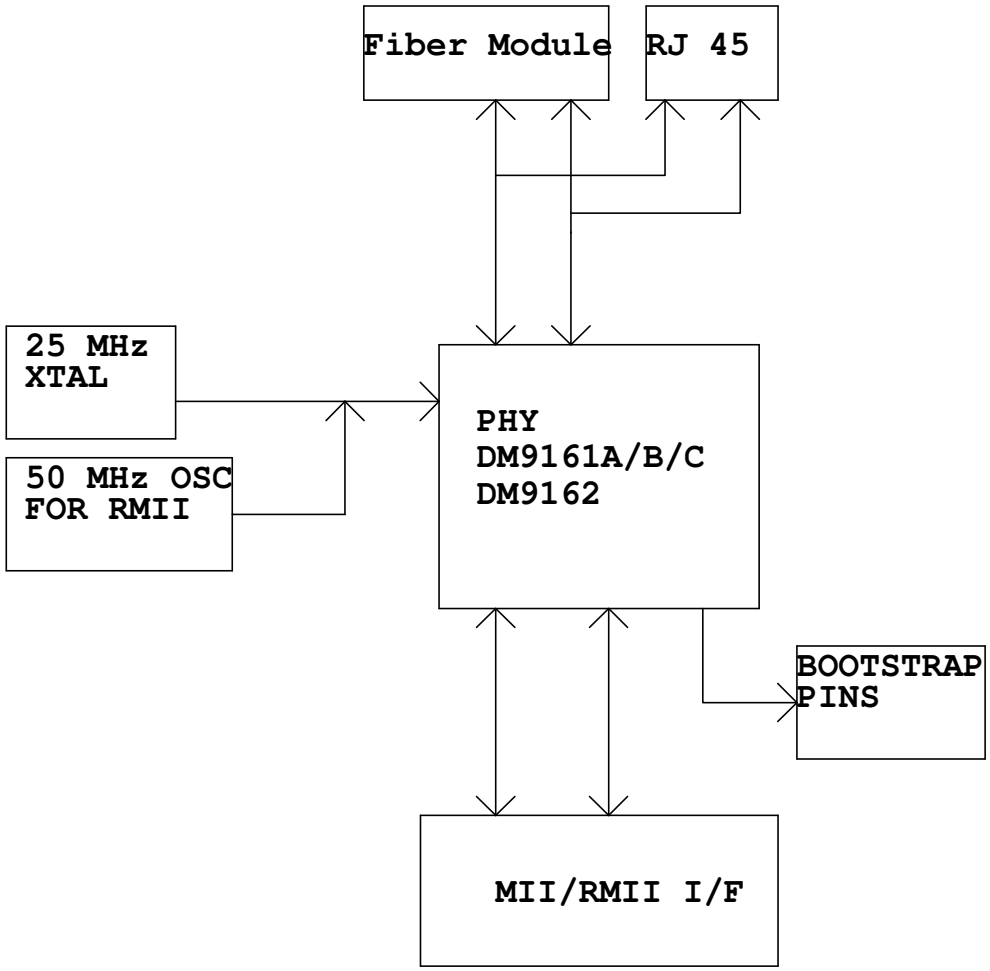

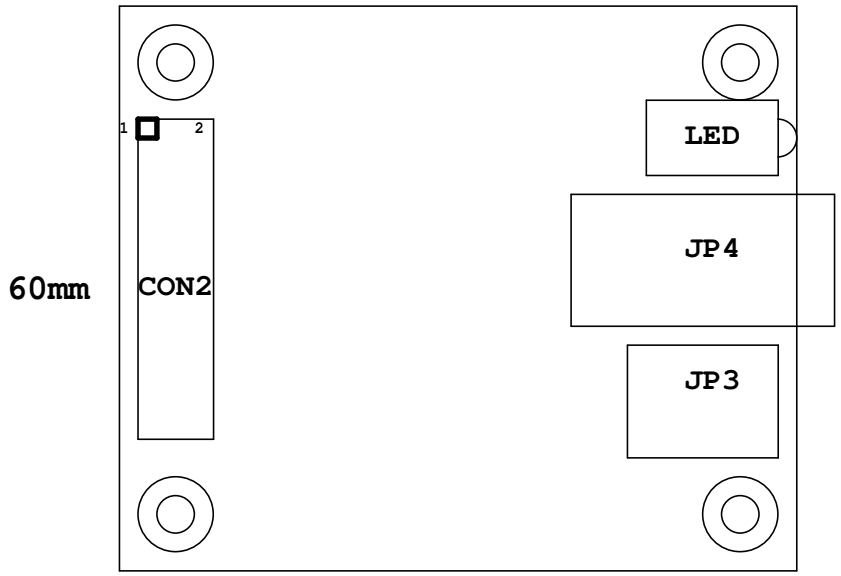

POWER FROM MII
+5V IN
+3.3V OUT
POWER
+3.3V IN
+1.8V OUT

Davicom Semiconductor Inc.		
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	MII/CRYSTAL	MII/OSCILLATOR	RMII/OSCILLATOR
R32	V	V	X
R33	V	V	X
R170	V	V	X
R34	V	V	X
R37	V	V	X
R38	V	V	X
R39	V	V	X
R40	V	V	X
R41	V	V	X
R43	X	X	V
R44	V	V	X
R45	V	V	X
R36	X	X	V
R47	X	X	V
R48	X	X	V
R49	X	V	X
R57	V	X	X
R58	V	X	X
Y3	V	X	X
Y2/Y4	X	V	V

X = DO NOT POPULATE
V = POPULATE

Y3 IS NEEDED FOR DM9162 WHEN
OUTPUT 50MHZ CLOCK ON TXCLK PIN

R35	R68	PHY ID
X	X	0
X	V	1
V	X	2
V	V	3

FOR DM9162, RMII
50MHZ CLOCK OUTPUT
AT TXCLK WHEN TXCLK
PULL-UP EXIST
DO NOT USE WITH ANY
OTHER PART

DM1961B SPEED LED MODIFICATION
ONLY NECESSARY FOR DM9161B
FOR OTHER PHY, DO NOT USE
TRANSISTOR

SELECT TP AND FIBER MODE:

OP0	OP1	OP2	
1	1	1	TP MODE
0	1	0	FIBER MODE

POWERDOWN
0 = NORMAL OPERATION
1 = POWERDOWN

PULL DOWN ONLY
FOR DEBUGGING
PURPOSE

AUTO-MDIX
0 = ENABLE
1 = DISABLE

Power 5V TO 3.3V

ADJUSTABLE LDO CALCULATION
Vout = Vref x (1 + RA2 / RA1)
Vref = 1.25 V
For fixed Vout LDO, RA1 = open,
RA2 = 0 ohm

Power 3.3V TO 1.8V

DO NOT USE

ADJUSTABLE LDO CALCULATION
Vout = Vref x (1 + RB2 / RB1)
Vref = 1.25 V
For fixed Vout LDO, RB1 = open,
RB2 = 0 ohm

RMII OSCILLATOR, 50MHZ:
RIVER FCXO-05 LF (TONSAM CORP)
SiTIME SiT8103AI-12-33E-50.00000

DGND COMBINE
WITH AGND, NO
GND PLANE
SEPARATION

power on reset
(select one use)

For FIBER MODULE

YT37-1107S

DAVICOM SEMICONDUCTOR INC.

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VER	DATE	ENGINEER	NOTE
1.0	12/12/2007	WILLIE NIOU	INITAL CIRCUIT CREATION
1.1	4/12/2010	WILLIE NIOU	BUG FIX AND ENHANCEMENTS: 1. CON2 GND CONNECT TO BOARD GND 2. LED LAYOUT LIBRARY NOT SAME AS ACUTAL COMPONENT USED. NEED TO CHANGE DIRECTION 180 DEGREES 3. C42 NEED TO CONNECT PIN 2 AND 3 TOGETHER 4. AGND AND DGND CONNECTED 5. ADD SPEED LED CONTROL CIRCUIT, DUE TO DM9161B DESIGN 6. ADD EXTERNAL 1.8V LDO FOR INPUT TO CENTER TAP OF TRANSFORMER TO REDUCE HEAT DISSIPATION BY CHIP
	2011/7/5	ALLIANG	1: ADD Fiber Module and termination circuit 2: CN2 MII Connector change to 16*2 Pinch 2.54mm 3: Change LED Anode & Cathode 4: Add R63,R80 For TXCLK and RXCLK wire link

Davicom Semiconductor Inc.

Title: PHY Demo Board (History)		
Size: A4	Document Number: HISTORY	Rev: 1.1
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