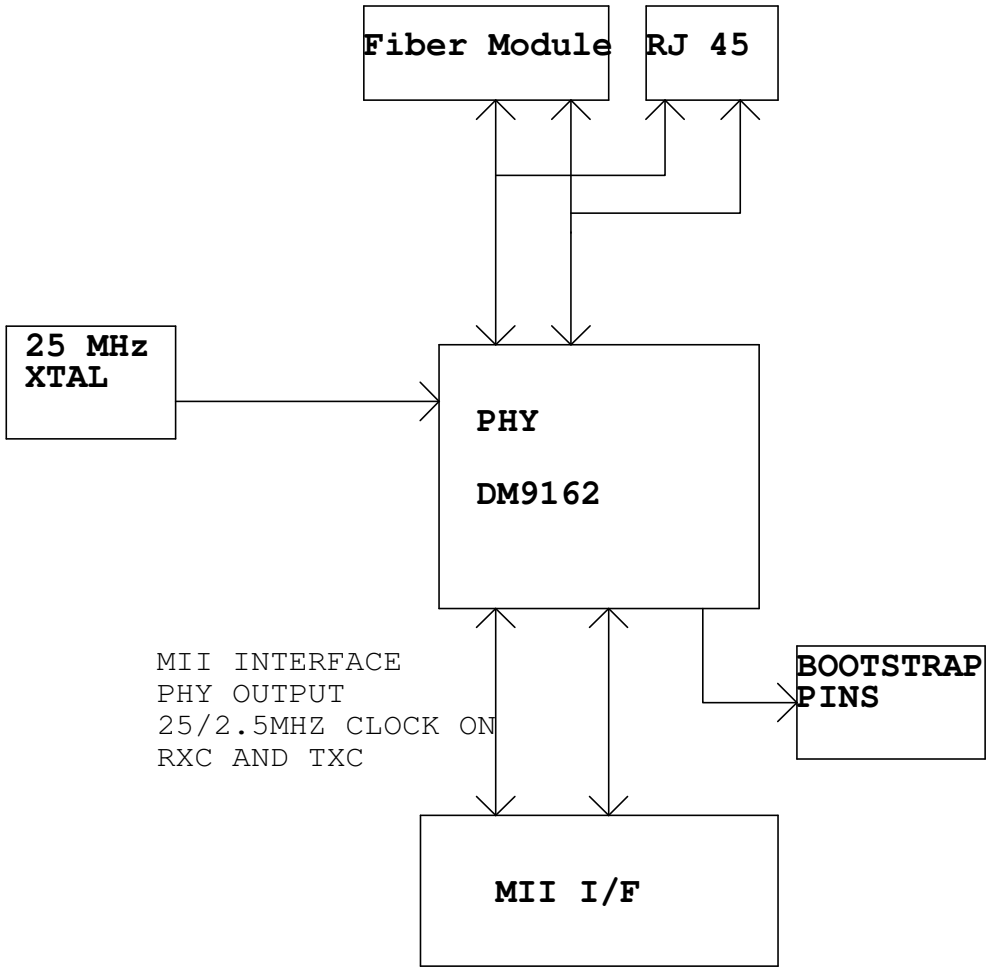

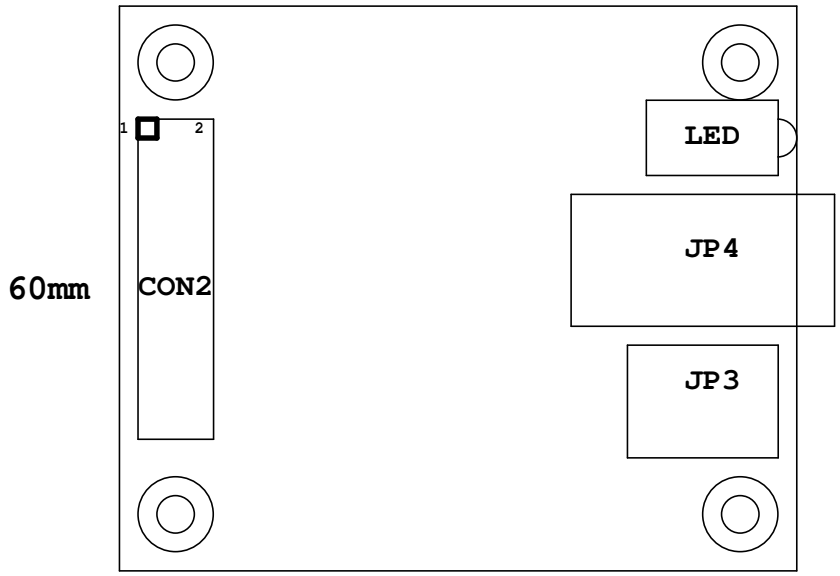

POWER FROM MII
+5V IN
+3.3V OUT
POWER
+3.3V IN
+1.8V OUT

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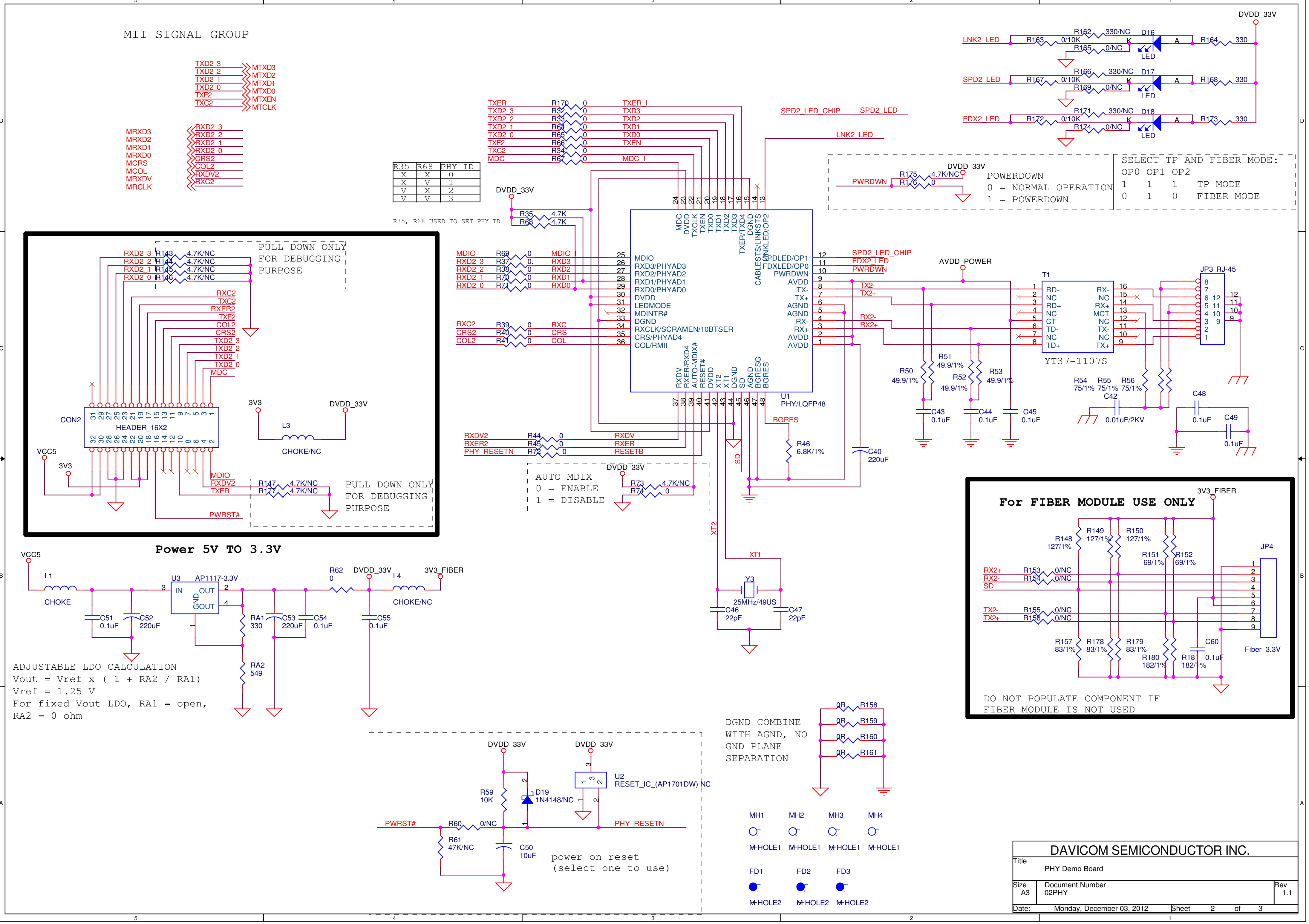
MII SIGNAL GROUP
TXD2_3 TXD2_2 TXD2_1 TXD2_0 TXE2 TXC2
MTXD3 MTXD2 MTXD1 MTXD0 MTXEN MTCLK
MRXD3 MRXD2 MRXD1 MRXD0 MCRS MCOL MRXDV MRCLK
RXD2_3 RXD2_2 RXD2_1 RXD2_0 CRS2 COL2 RXDV2 RXC2
R35 R68 PHY ID
X X 0
X V 1
V X 2
V V 3
R35, R68 USED TO SET PHY ID
PULL DOWN ONLY FOR DEBUGGING PURPOSE
CON2 HEADER_16X2
3V3 DVDD_33V L3 CHOKE/NC
VCC5
AUTO-MDIX
0 = ENABLE
1 = DISABLE
U1 PHY/LQFP48
MDIO RXD3/PHYAD3 RXD2/PHYAD2 RXD1/PHYAD1 RXD0/PHYAD0 DVDD LEDMODE MDINTR# DGND RXCLK/SCRAMEN/10BTSER CRS/PHYAD4 COL/RMII
SPDLED/OP1 FDXLED/OP0 PWRDWN AVDD TX- TX+ AGND AGND RX- RX+ AVDD AVDD
SPD2_LED_CHIP FDX2_LED PWRDWN AVDD_POWER
T1 YT37-1107S
JP3 RJ-45
LNK2_LED SPD2_LED FDX2_LED D16 D17 D18 LED
POWERDOWN
0 = NORMAL OPERATION
1 = POWERDOWN
SELECT TP AND FIBER MODE:
OP0 OP1 OP2
1 1 1 TP MODE
0 1 0 FIBER MODE
For FIBER MODULE USE ONLY
3V3_FIBER JP4 Fiber_3.3V
DO NOT POPULATE COMPONENT IF FIBER MODULE IS NOT USED
Power 5V TO 3.3V
U3 AP1117-3.3V L1 CHOKE L4 CHOKE/NC
ADJUSTABLE LDO CALCULATION
Vout = Vref x (1 + RA2 / RA1)
Vref = 1.25 V
For fixed Vout LDO, RA1 = open,
RA2 = 0 ohm
Y3 25MHz/49US
DGND COMBINE WITH AGND, NO GND PLANE SEPARATION
U2 RESET_IC_(AP1701DW) NC
D19 1N4148/NC
PWRST# PHY_RESETN
power on reset
(select one to use)
MH1 MH2 MH3 MH4 M-HOLE1
FD1 FD2 FD3 M-HOLE2
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VER	DATE	ENGINEER	NOTE
1.0	12/12/2007	WILLIE NIOU	INITAL CIRCUIT CREATION
1.1	4/12/2010	WILLIE NIOU	BUG FIX AND ENHANCEMENTS: 1. CON2 GND CONNECT TO BOARD GND 2. LED LAYOUT LIBRARY NOT SAME AS ACUTAL COMPONENT USED. NEED TO CHANGE DIRECTION 180 DEGREES 3. C42 NEED TO CONNECT PIN 2 AND 3 TOGETHER 4. AGND AND DGND CONNECTED 5. ADD SPEED LED CONTROL CIRCUIT, DUE TO DM9161B DESIGN 6. ADD EXTERNAL 1.8V LDO FOR INPUT TO CENTER TAP OF TRANSFORMER TO REDUCE HEAT DISSIPATION BY CHIP
	2011/7/5	ALLIANG	1: ADD Fiber Module and termination circuit 2: CN2 MII Connector change to 16*2 Pinch 2.54mm 3: Change LED Anode & Cathode 4: Add R63,R80 For TXCLK and RXCLK wire link

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