CIRRUS LOGIC®

Application Note

Crystal LAN™ CS8900A ETHERNET CONTROLLER TECHNICAL REFERENCE MANUAL

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SCHEMATIC CHECKLIST

Before getting into the meat of the technical reference manual here is a schematic checklist. It's presented here, at the beginning, to help the hardware designer implement the design quickly and easily.

- No caps across the crystal. The CS8900A implements these internally.
- 4.99K 1% resistor between pin 93 and pin 94. A common mistake is the resistor is connected to Vcc instead of ground.
- RESET is active high, not active low.
- Check addressing.
- On non-ISA systems, if the processor is Big Endian, it may be beneficial to byte swap the data lines to minimize byte swapping in software.
- SBHE (16 bit mode) -- must be low on IO or Mem address. And it must toggle at least once to put the CS8900 in 16 bit mode.
- IO and Memory Accesses: SBHE, AEN, etc. must be stable for 10ns (read) and 20ns (write) before access.
- IOCHRDY - Generally not connected in non-ISA bus.
- CHIPSEL (active low). Tie to ground if not using ELCS.
- Make sure interrupt line is active high. It is best to put a pull down (10K) on INT line since selected IRQ line is tristated during software initiated reset.
- ELCS should be pulled to ground or left floating if not used.
- EEDataIn should be pulled to ground if not used.
- 10Base-T circuit -- no caps on TX lines between isolation transformer and 10 Base-T connector.
- 10Base-T circuit -- no center tap caps on isolation transformer and 10 Base-T connector. Good to have pads, don't populate except for EMI problems.
- Isolation transformer -- start with one that does not have a common mode choke. If there are EMI considerations, then use one with common mode choke. The pin outs are the same. For 3.3V operation, use a transformer with 1:2.5 turns ration on TX and 1:1 on RX like the YL18-1080S.
- For EMI problems, 1) add choke, 2) add center tap caps on isolation transformer
- If using a shielded RJ45 connector, make sure the shield pins are connected to chassis ground.
- AEN connected to ground if not using DMA.
- AEN can be used as an active low chip select if not using DMA.
- AUI Interface -- use a 1AMP fuse. MAU can use .5amps even better use a thermistor ("poly switch"). Also, use a diode so can't back-drive from an externally powered MAU. Use a Halo TnT integrated module to simplify 10Base2 interface.
- TX series termination resistors are R: 24.3 Ohm 1% (8 or 8.2 Ohm 1% for 3.3V)
- RX shunt termination resistor is 100 Ohm
- Put a 68pF shunt across TX on primary side (560pF for 3.3V)
- Don't use split analog/digital power and ground planes.
- Void ground/power plane from transformer to RJ45
- Put .1uF cap on each supply pin very close to CS8900

The schematic checklist and the example connection diagrams to the Hitachi SH3, Cirrus Logic CL-PS7211 and the Motorola MC68302 microprocessors should make clear the necessary the hardware connections for a wide variety of situations.

INTRODUCTION TO CS8900A TECHNICAL REFERENCE MANUAL

This Technical Reference Manual provides the information which will be helpful in designing a board using the CS8900A, programming the associated EEPROM, and installing and running the CS8900A device drivers. It is expected that the user of this technical reference manual will have a general knowledge of hardware design, Ethernet, the ISA bus, and networking software. Recommended sources of background information are:

ISA System Architecture by Shanley and Anderson, Mindshare Press, 1992, ISBN 1-881609-05-7

Ethernet, Building a Communication Infrastructure, by Hegering and Lapple, Addison-Wesley, 1993, ISBN 0-201-62405-2

Netware Training Guide: Networking Technologies, by Debra Niedenmiller-Chaffis, New Riders Publishing, ISBN 1-56205-363-9

As shown in the Figure 1, the CS8900A requires a minimum number of external components. The EEPROM stores configuration information such as interrupt number, DMA channel, I-O base address, memory base address, and IEEE Individual Address. The EEPROM can be eliminated on a PC motherboard if that information in stored in the system CMOS. Note also that the Boot PROM is only needed for diskless workstations that boot DOS at system power up, over the network. Also, the LEDs are optional.

The hardware design considerations for both motherboards and adapter cards are discussed in "HARDWARE DESIGN" on page 7. The EEPROM programming considerations are described in "JUMPERLESS DESIGN" on page 45.

Cirrus provides a complete set of device drivers, as discussed in "DEVICE DRIVERS AND SETUP/INSTALLATION SOFTWARE" on page 56. The drivers reside between the networking operating system (NOS) and the CS8900A. On the CS8900A side, the drivers understand how to pro-

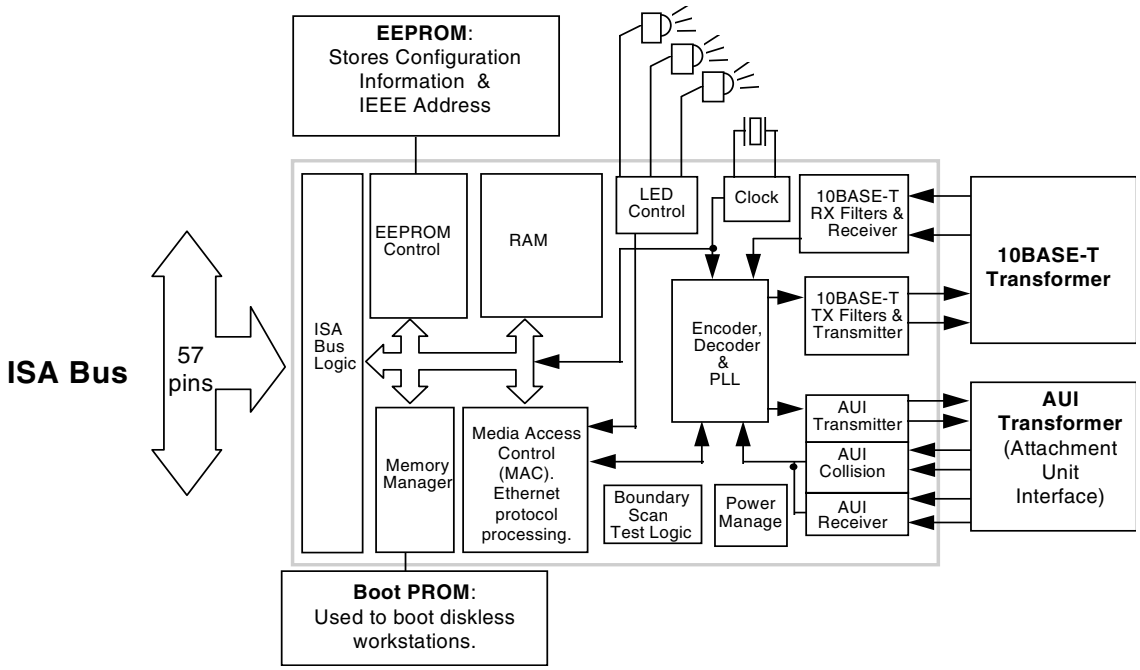

Figure 1. Hardware Application Summary

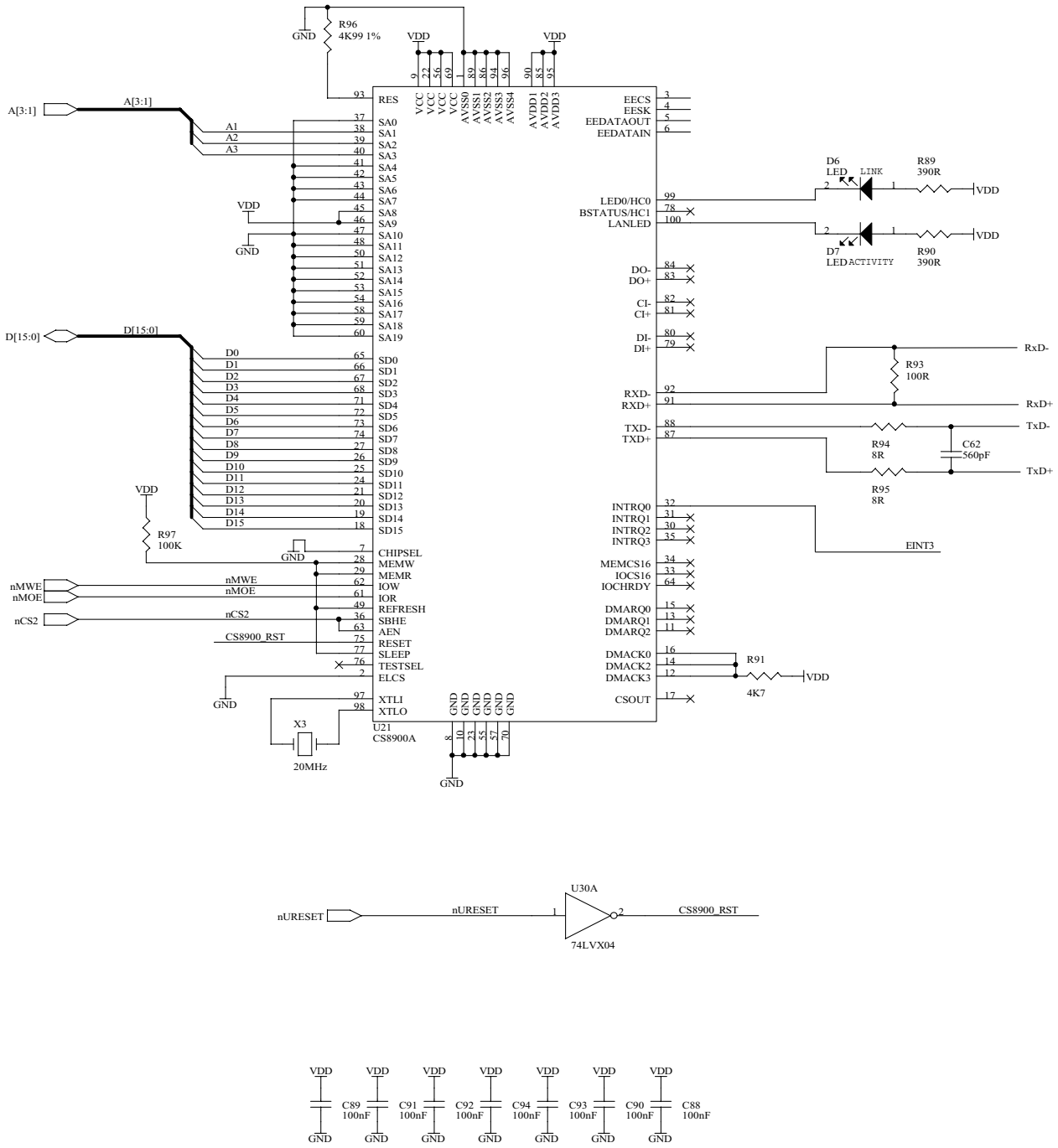

Figure 4. CS8900A Interface to Cirrus Logic CL-PS7211

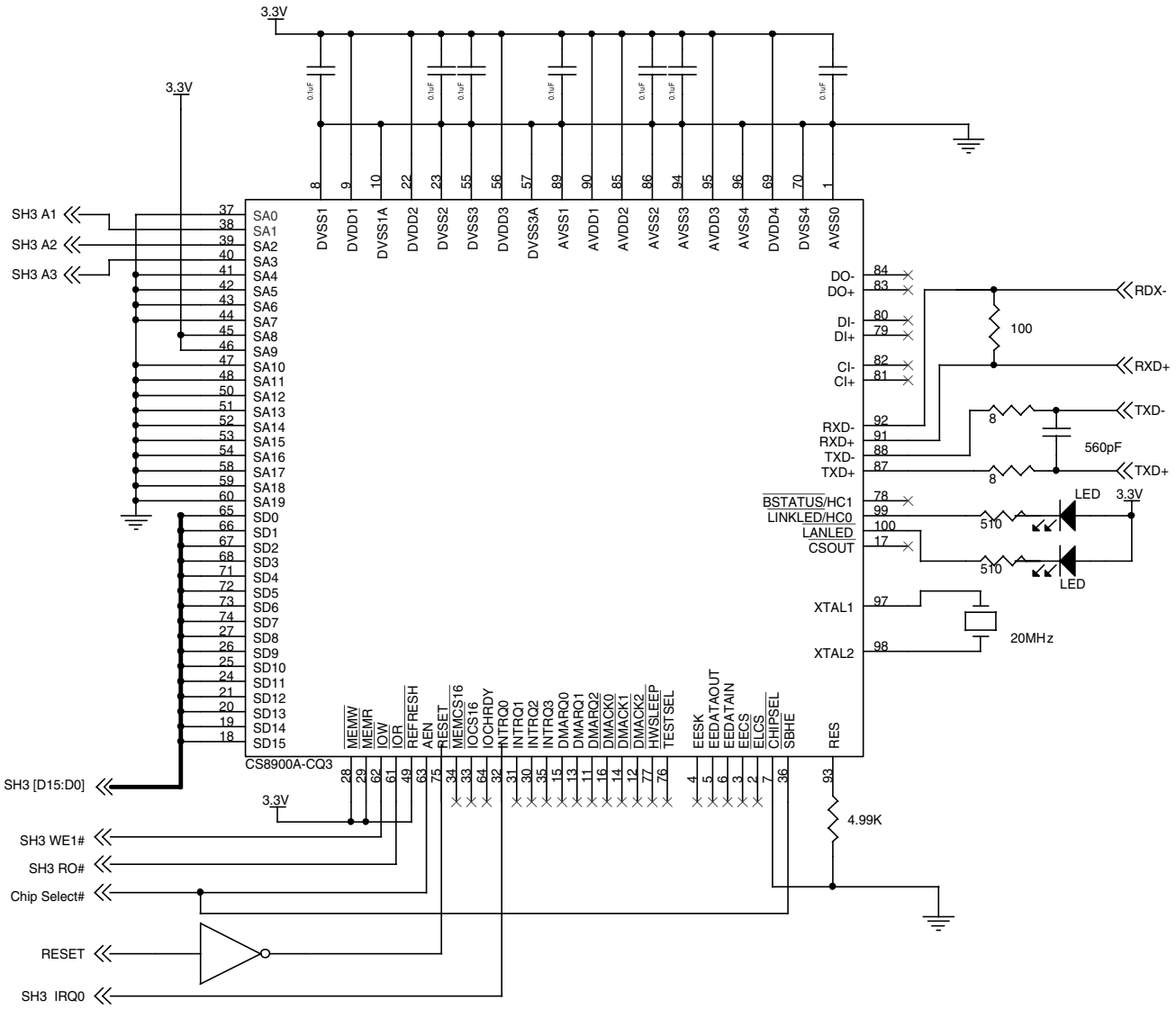

Figure 5. CS8900A Interface to Hitachi SH3

PROM is not necessary for the CS8900A, and the CS8900A will respond to IO addresses 0300h through 030Fh after a reset.

Please refer to the CS8900A data sheet for information about programming the EEPROM. Please refer to "JUMPERLESS DESIGN" on page 45 of this document for information about EEPROM internal word assignments.

LEDs

Many embedded systems do not require LEDs for the Ethernet traffic. Therefore this reference design does not implement any LEDs. However, the CS8900A has direct drives for the three LEDs. Please refer to the data sheet for the CS8900A for a description of the LED functions available on the CS8900A.

10BASE-T Interface

The 10BASE-T interface for the CS8900A is straight forward. Please refer to Figure 8 (3.3V) and Figure 10 (5V) for connections and components of this circuit. Transmit and receive signal lines from the CS8900A are connected to an isolation transformer at location T1. This isolation transformer has a 1:1 ratio between the primary and the secondary windings on the receive side. It has a 1:√2 (1:1.414) ratio between the primary and the secondary windings for the transmit lines for 5V operation or a ratio of 1:2.5 for 3.3V operation. Resistor R1 provides termination for the receive lines. Resistors R2 and R3 are in series with the differential pair of transmit lines for impedance matching.

10BASE-2 and AUI Interfaces

As many embedded systems require only a 10BASE-T interface, this reference design implements only the 10BASE-T interface. However, should a user require a 10BASE-2 or AUI interface, the CS8900A provides a direct interface to the AUI. Please refer to "Low Cost Ethernet Combo Card Reference Design: CRD8900" on page 21 of this document for details about the AUI interface.

Logic Schematics

Figures 8, 9 and 10 detail the logic schematics for the various circuits used in the reference design.

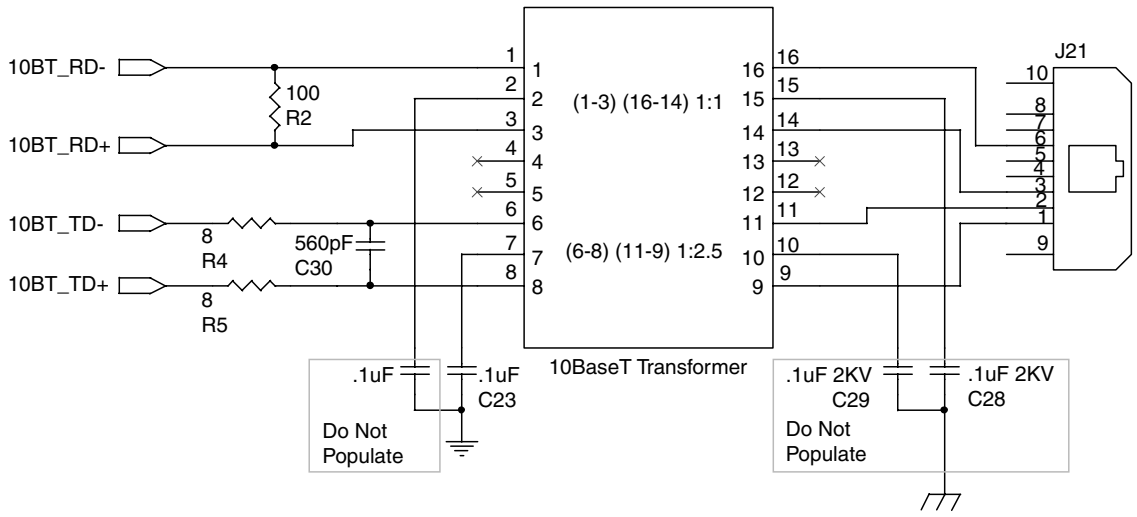

Figure 8. 10BASE-T Schematic 3.3V

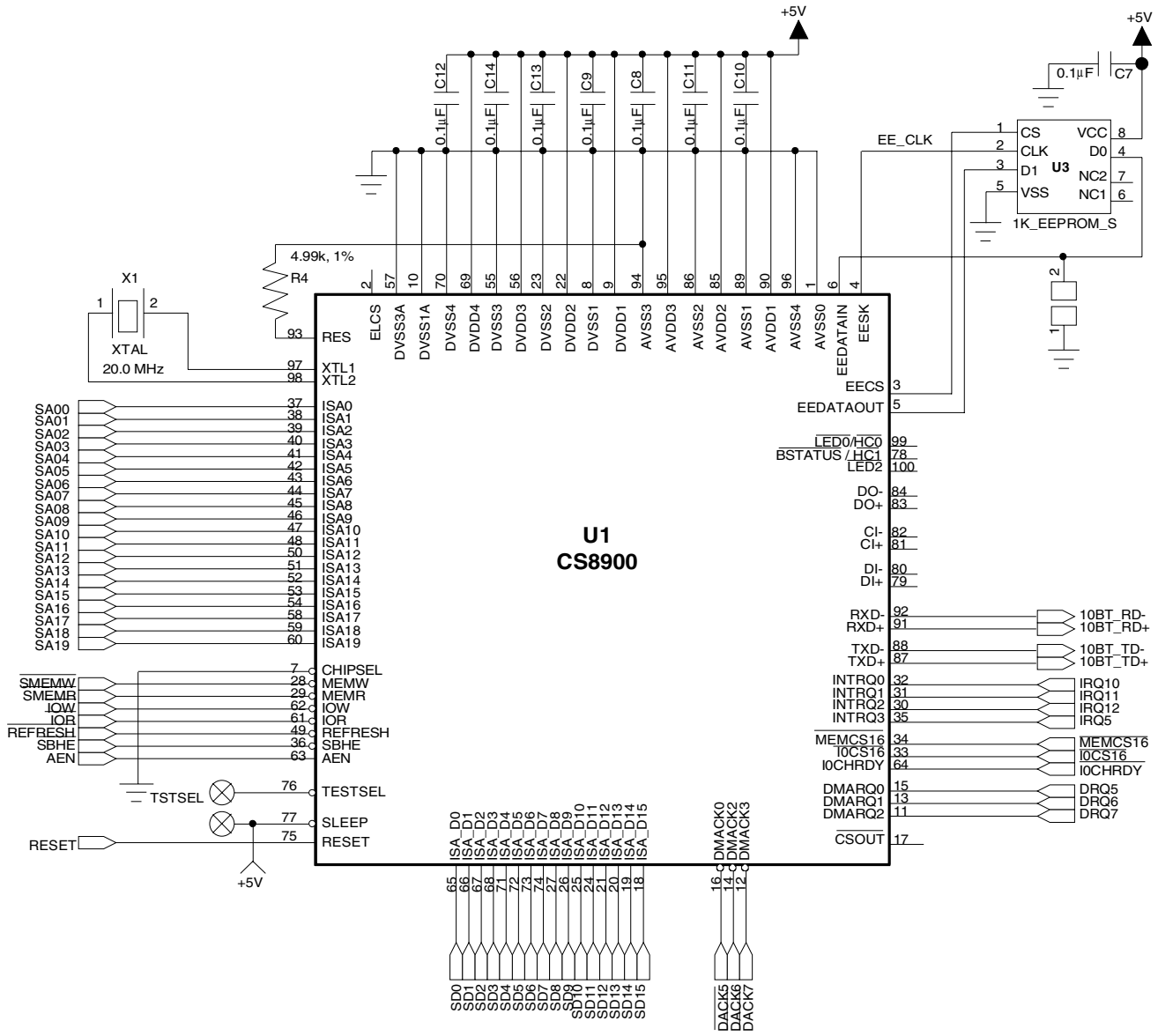

Figure 9. Overall Schematic

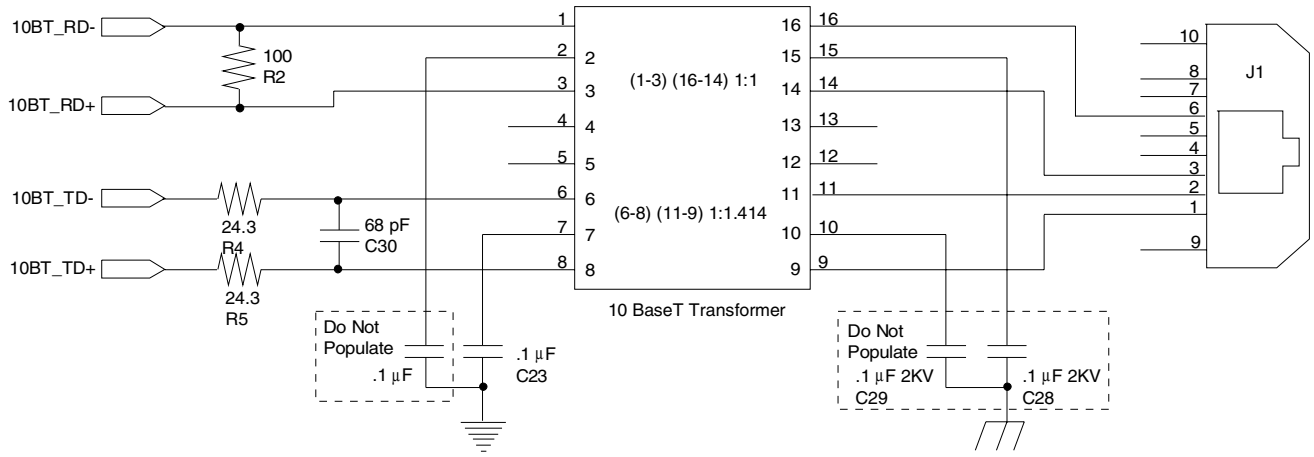

Figure 10. 10BASE-T Schematic 5V

Component Placement and Signal Routing

Please refer to "Layout Considerations for the CS8900A" on page 35 of this document for more details on the placement of components on the board. It is important to provide very clean and adequate +5 V and ground connections to the CS8900A.

Bill of Material

Table 1 has a list components that are typically used to assemble this adapter card. For most of the components, there are several alternative manufacturers.

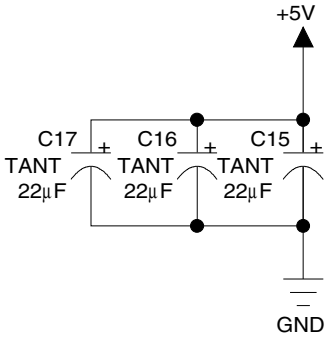

Figure 11. Decoupling Capacitors Schematic

Item	Reference #	Description	Quantity	Vendor	Part Number
1	C2, C5, C7..C14	Capacitor, 0.1 µF, X7R, SMT0805	10		
2	C15, C16, C17	Capacitor, 22 µF, SMT7343	3		
3	R2, R3	Resistor, 24.3, 1%, 1/8W, SMT0805	2		
4	R1	Resistor, 100, 1%, 1/8W, SMT0805	1		
5	R4	Resistor, 4.99K, 1%, SMT0805	1		
6*	X1	Crystal, 20.000 MHz	1	M-tron	ATS-49,20.000 MHz,18 pF
7	J1	Connector, RJ45, 8 pin	1	AMP	555164-1
8	T1	Transformer,2,1:1,1:1.41	1	YUTAI	YL18-1064S
9	U1	ISA Ethernet Controller	1	Crystal	CS8900A
10*	U3	1K EEPROM	1	Microchip	93C46 (8 pin SOIC)

* Depending on system resources, these parts may not be needed.

Table 1. CS8900A Design Bill of Materials

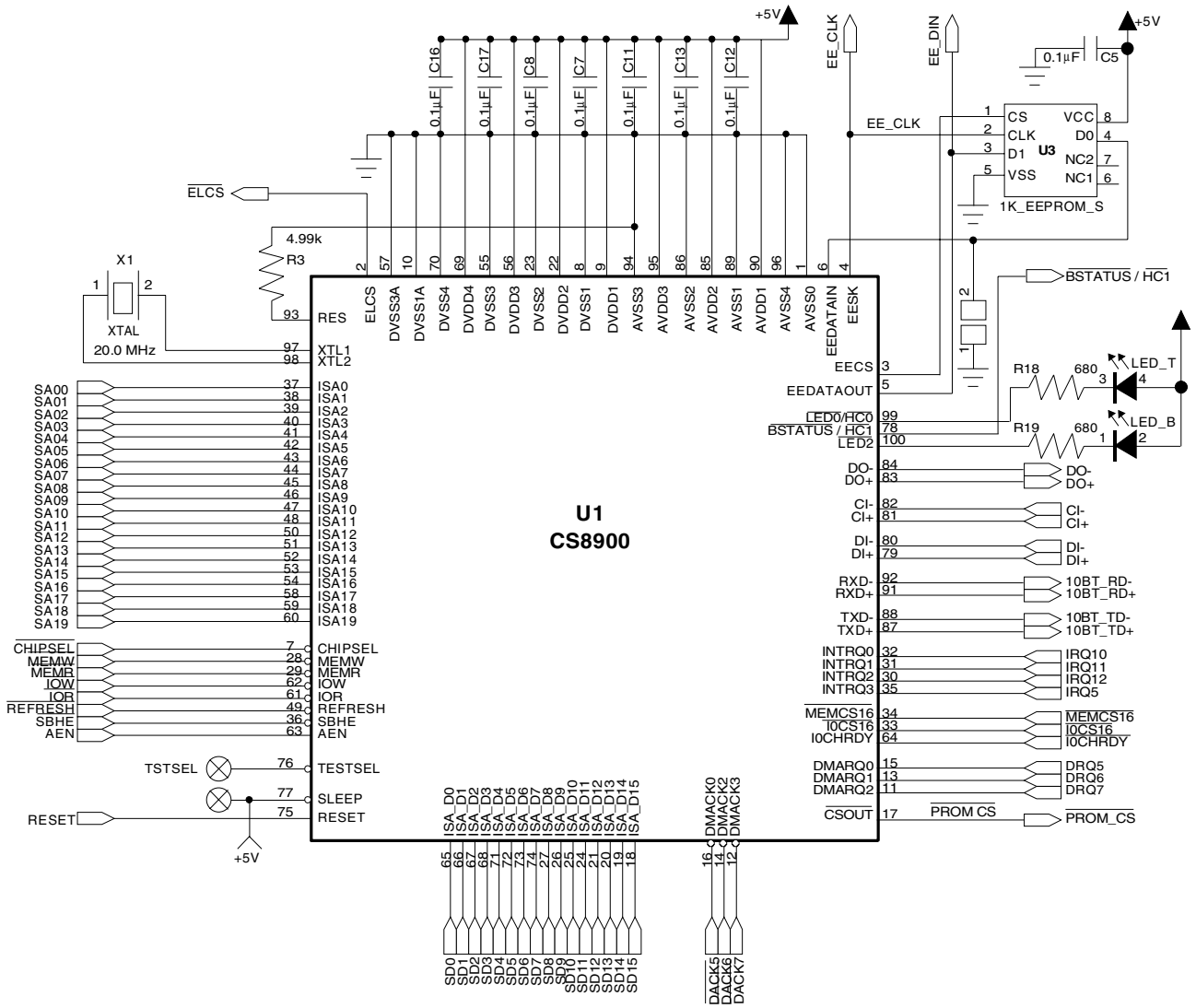

Figure 13. CS8900A Schematic (Combo Card Application)

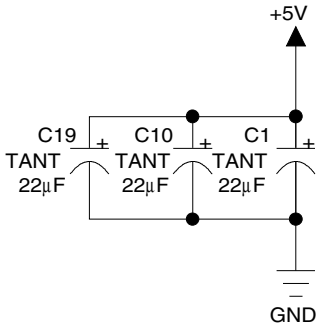

Figure 14. Power Supply Decoupling Schematic

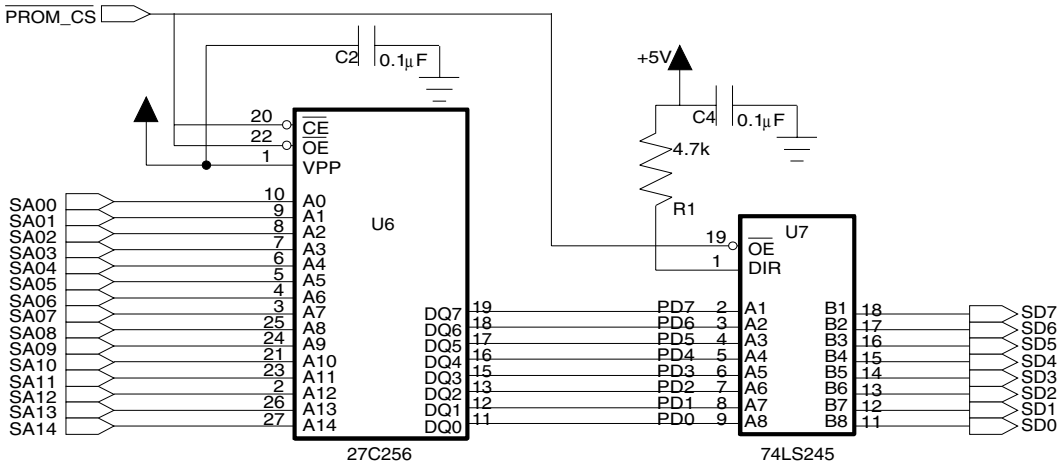

Figure 15. Boot PROM Schematic

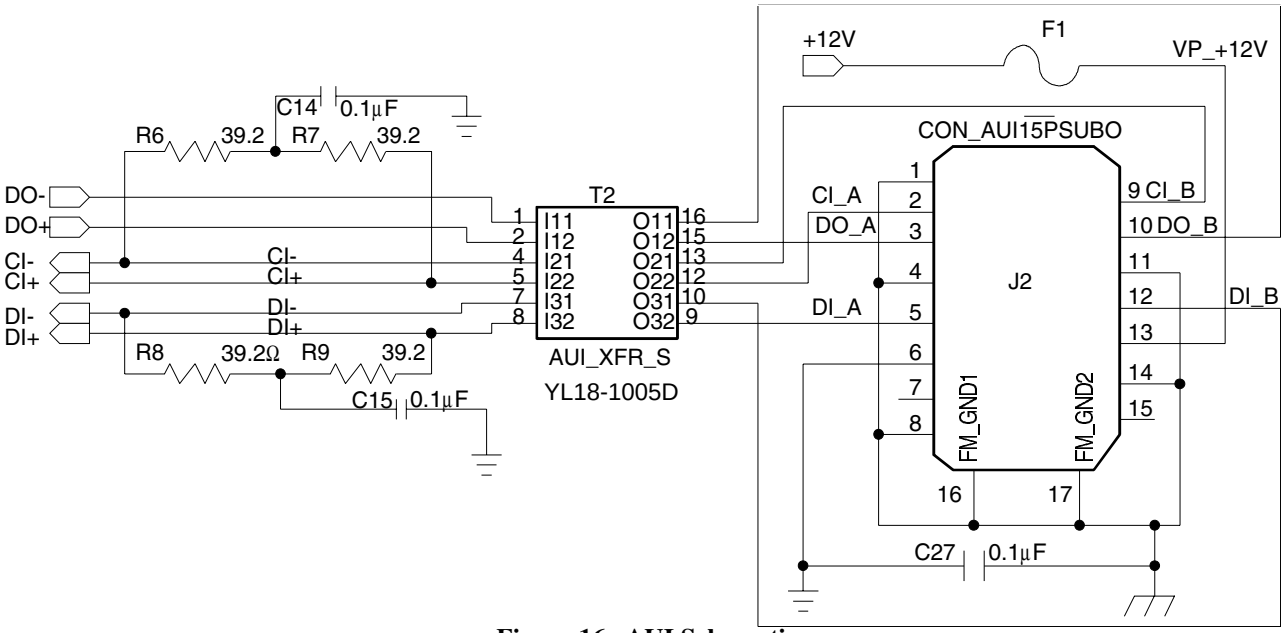

Figure 16. AUI Schematic

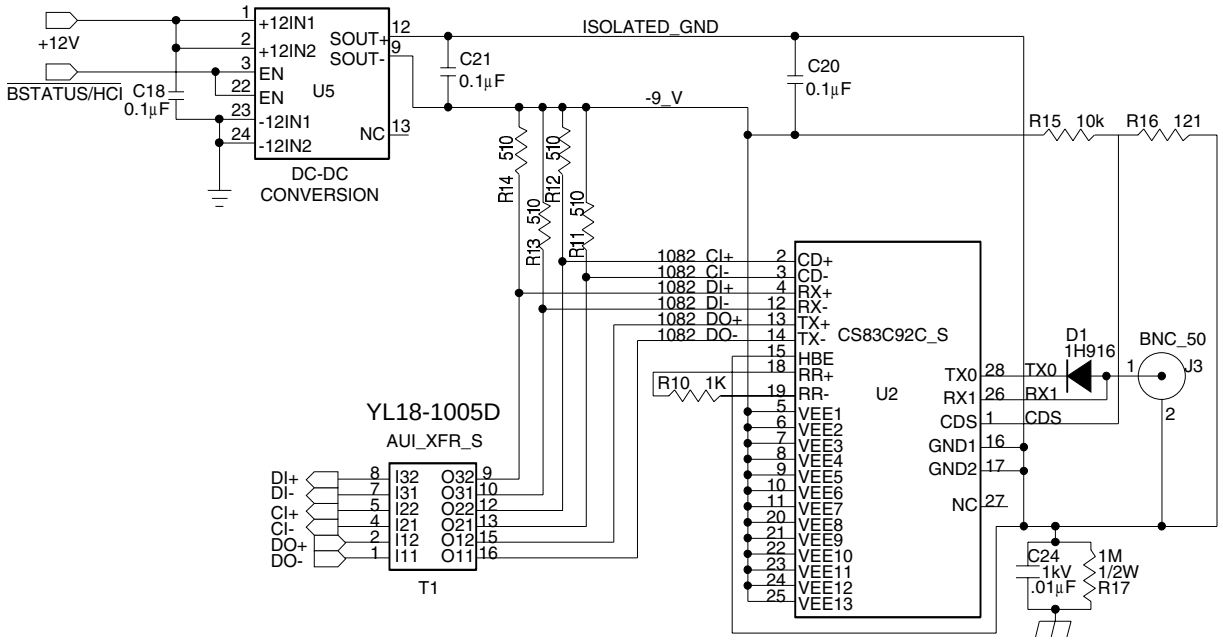

Figure 17. 10BASE-2 Schematic

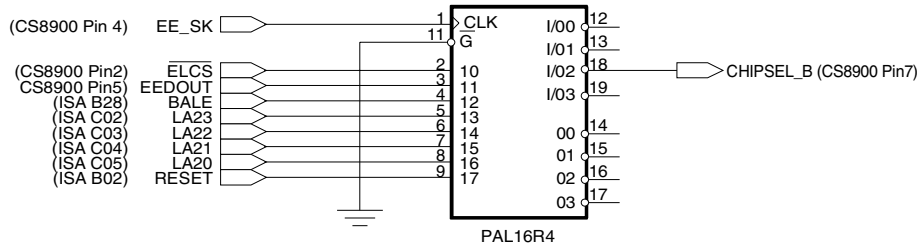

Figure 18. PAL Decode of LA[20-23]