


LAN9500i/LAN9500Ai Reference Design

Schematic Revision 2.4

Circuit Diagrams utilizing SMSC Products Are Included As A Means Of Illustrating Typical Semiconductor Applications: Consequently Complete Information Sufficient For Construction Purposes Is Not Necessarily Given. The Information Has Been Carefully Checked And Is Believed To Be Entirely Reliable. However, No Responsibility Is Assumed For Inaccuracies. Furthermore, Such Information Does Not Convey To The Purchaser Of The Semiconductor Devices Described Any License Under The Patent Rights Of SMSC Or Others. SMSC Reserves The Right To Make Changes At Any Time In Order To Improve Design And Supply The Best Product Possible.

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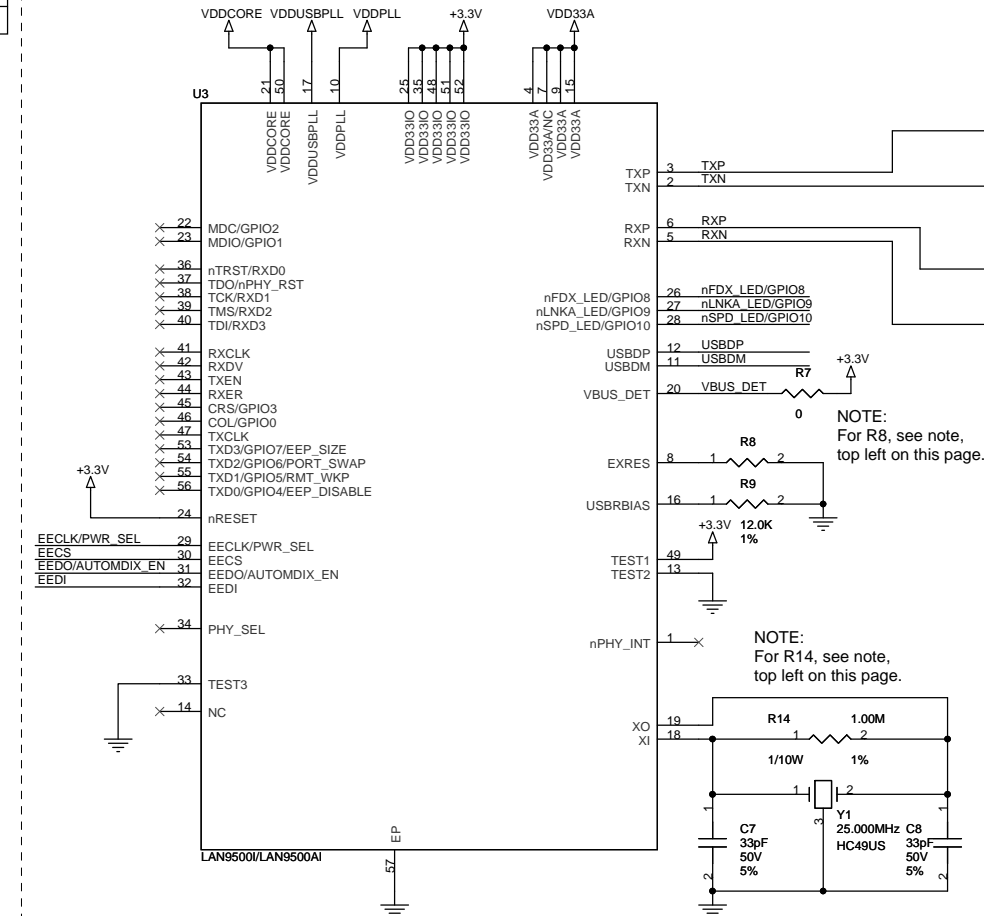
			
Title: LAN9500i/LAN9500Ai Reference Design			
Size: C	Engineer: R.W.	Assembly No.: LAN9500i/LAN9500Ai	Rev: 2.4
Date: Thursday, December 10, 2009		Sheet 1 of 2	

NOTE:
Populate R6, R8 and R14 according to table below.

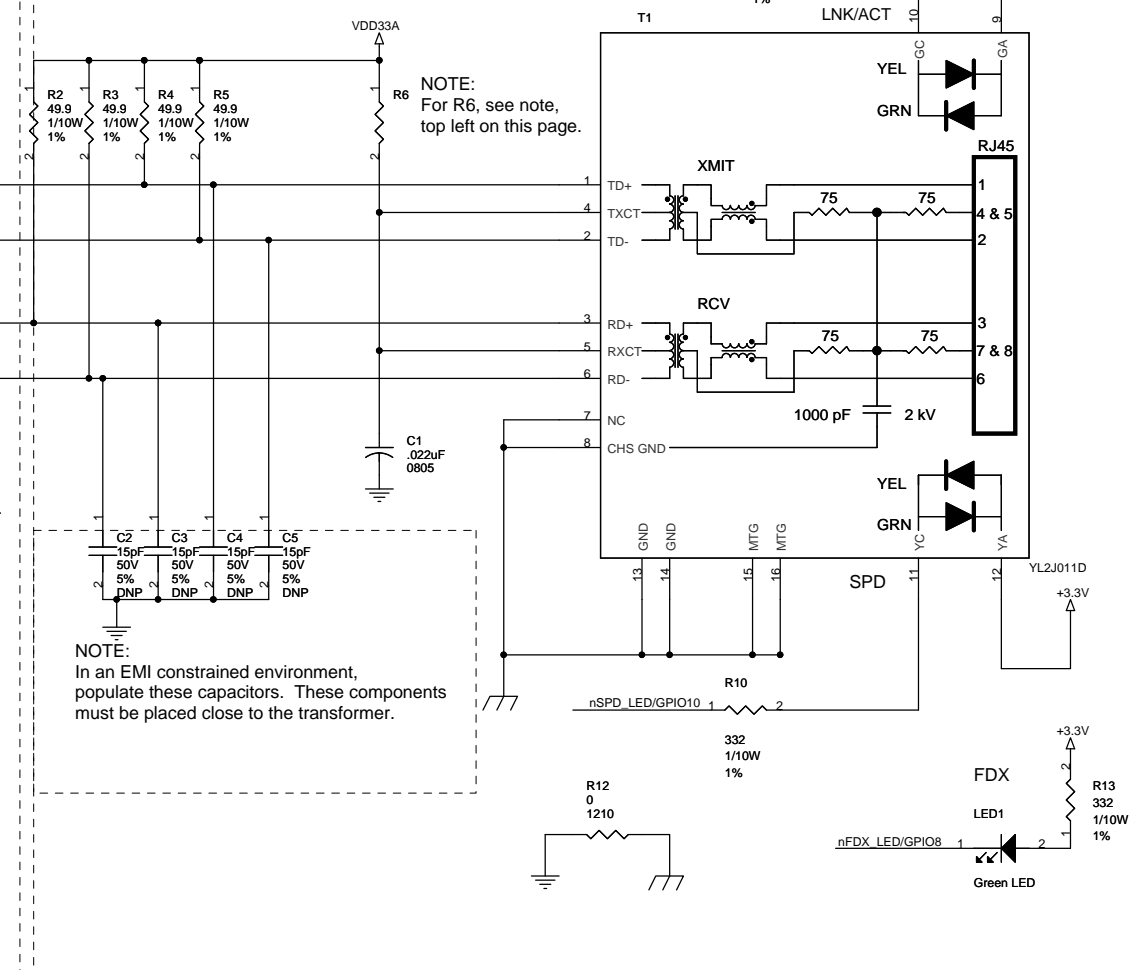
U3	R6	R8	R14
LAN9500i	10 ohm 1%	12.4K 1%	1.0 M 1%
LAN9500Ai	0 ohm	12.0K 1%	DNP

NOTE:
Pin 7 is a no-connect (NC) for LAN9500Ai, but may be connected to VDD33A for backward compatibility with LAN9500i designs.

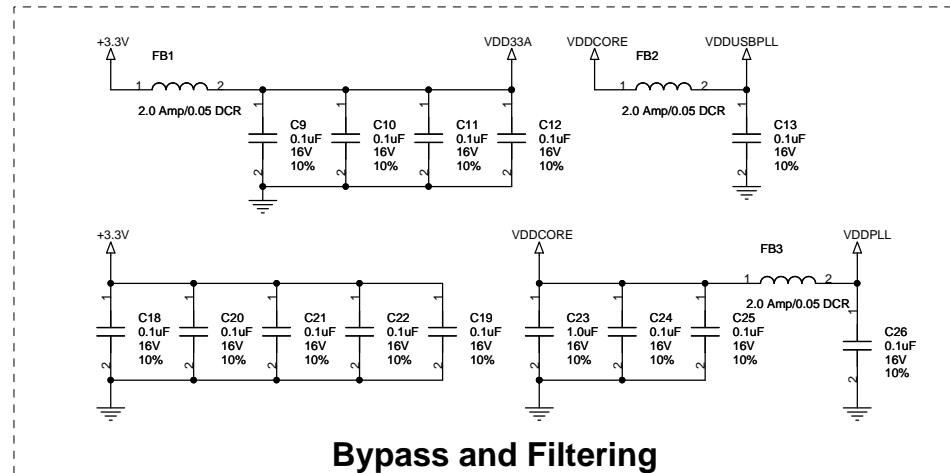
NOTE:
Place R2-R5 near LAN9500Ai.
Place R6 and C1 near transformer.



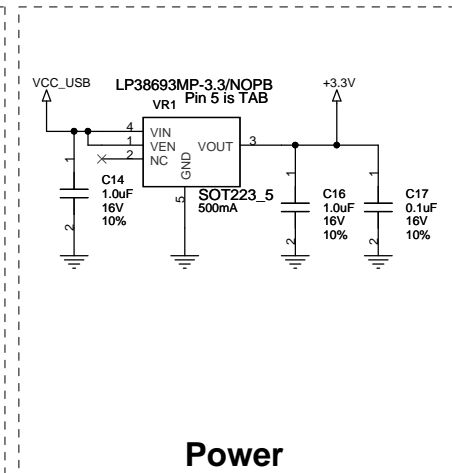
LAN9500i/LAN9500Ai



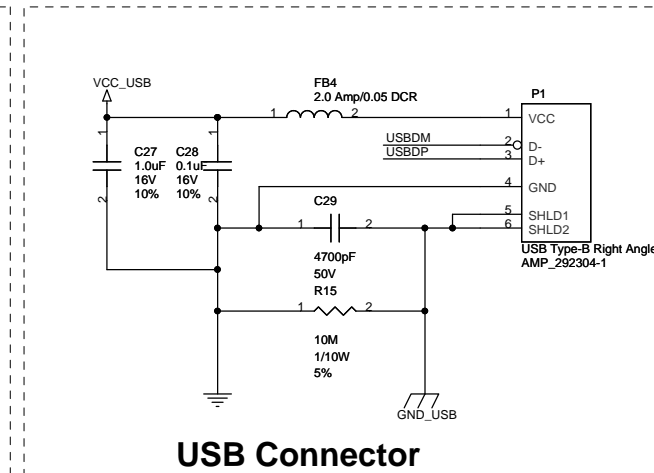
Ethernet



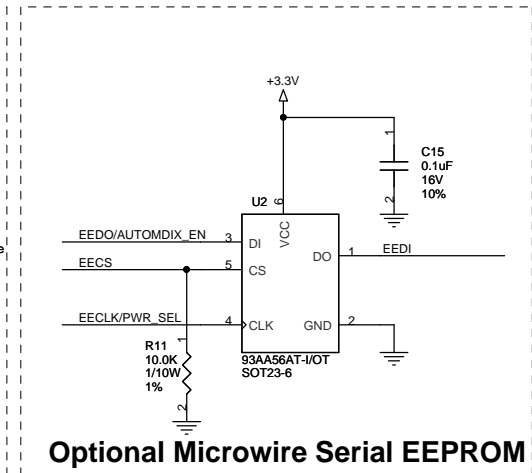
Bypass and Filtering



Power



USB Connector



Optional Microwire Serial EEPROM