

AX88180 RTL8251CN RGMII GigaPHY Reference Schematic Index

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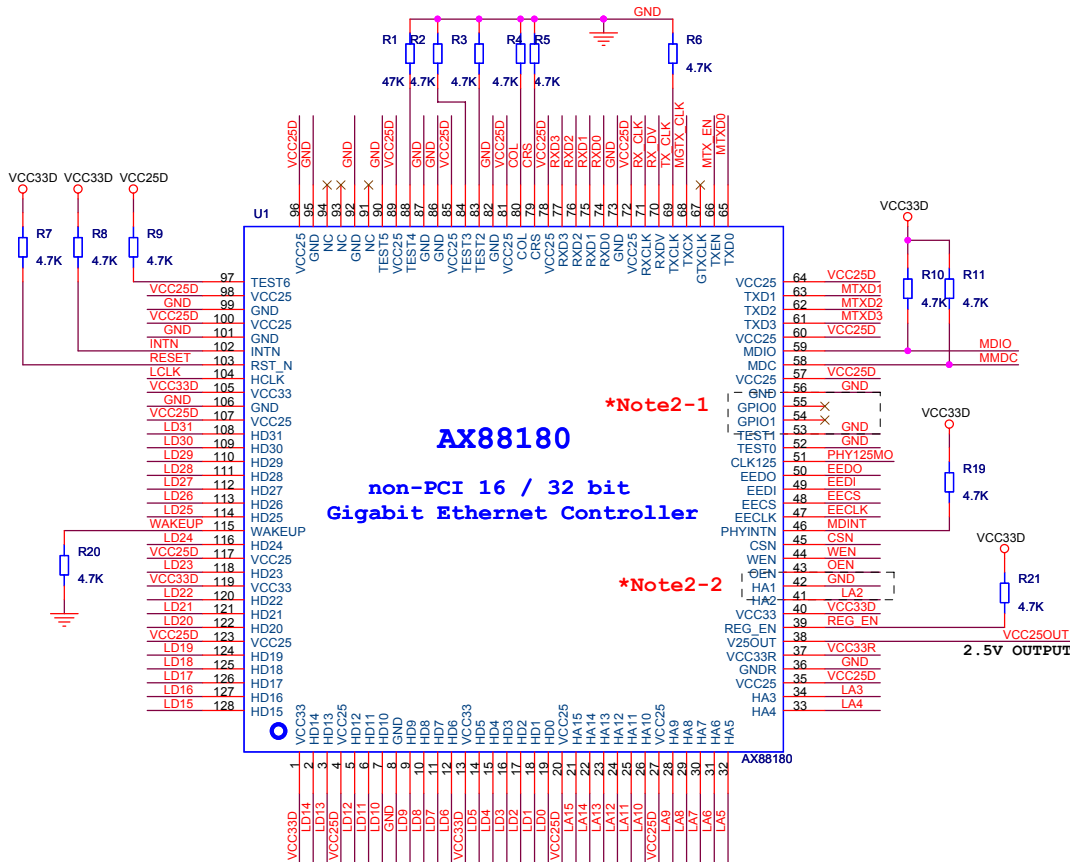
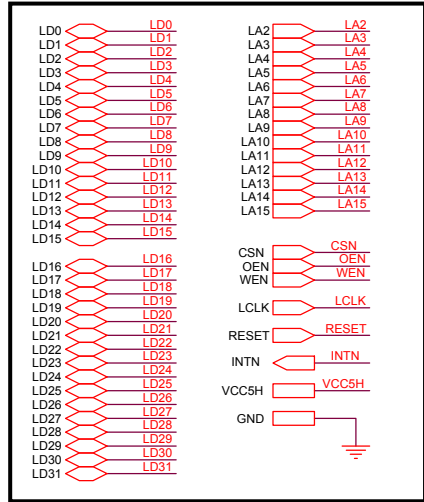
Page3:
RTL8251CN GigaPHY
25MHz Crystal
Power Circuit

Note:

1. Please refer to AX88180 Gigabit Ethernet Controller Application Design Note for more AX88180 PCB layout design notes.
2. Please contact ASIX Support (support@asix.com.tw) to get AX88180 EEPROM User Guide for more details about AX88180 EEPROM setting.
3. Please deliver us your AX88180 schematic and your AX88180 EEPROM data file for further review.
4. Please contact Realtek's support guys to get the latest RTL8251CN reference schematic and Layout Guide and further suggestions before making your PCB board.

ASIX ELECTRONICS CORPORATION				
Title				
System Block				
Size	Document Number			Rev
B	AX88180+GigaPHY RTL8251CN Reference Schematic			V1.00
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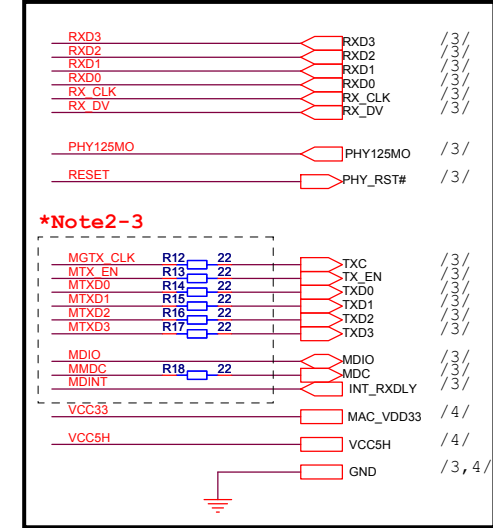
Host Interface Connection



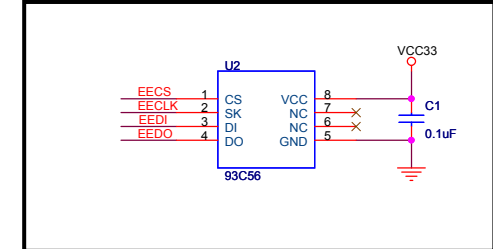
*Note2-1

*Note2-2

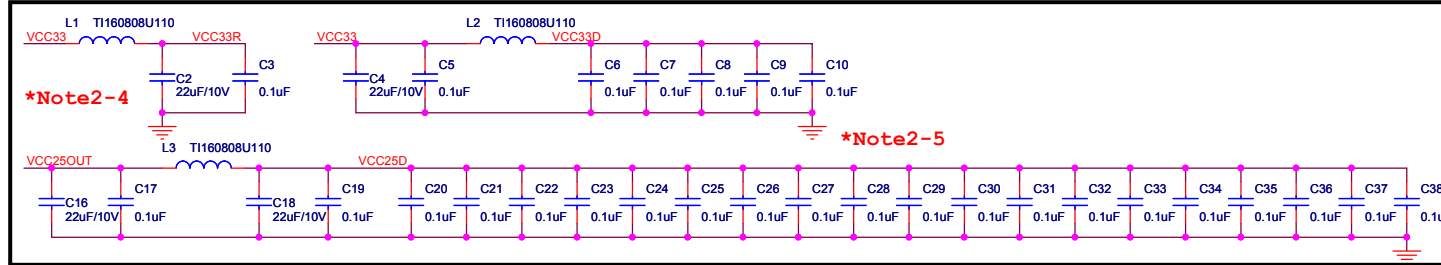
RG MII interface



93C56 EEPROM



AX88180 Power 3.3V and 2.5V By Pass



***Note2-1**
AX88180 Mode Configure:
GPIO 0 : Pull-up : 16-bit mode
Pull-down (Default) : 32-bit mode
GPIO 1 : Pull-up : Big Endian
Pull-down (Default) : Little Endian
GPIO 0/GPIO 1 are pulled down by hardware default

***Note2-2**
The HA1 pin should be connected to GND when the MCU is set to the double-word boundary mode. Please refer to Appendix A2 of AX88180 datasheet for more details.

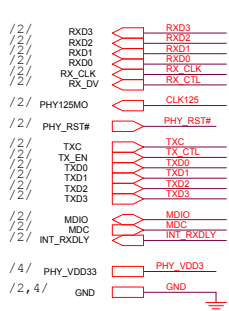
***Note2-3**
These 22 Ohm terminal resistors should be as close to AX88180's MII interface

***Note2-4**
The L1 should be kept the trace wider than 46mils for good power regulation. The VCC33R signal should be wider than 40mils on regulator input trace and C2 as close to VCC33R for good power regulation. The VCC25OUT signal should be wider than 20mils and C18 as close to V25OUT for good power regulation.

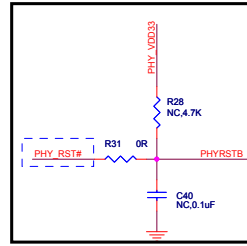
***Note2-5**
Every by-pass capacitors should be as close to each power pins to reduce high frequency power noises.

AX88180
32 Bit / RG MII Mode
Little Endian

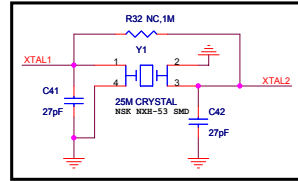
ASIX ELECTRONICS CORPORATION		
Title AX88180		
Size	Document Number	Rev
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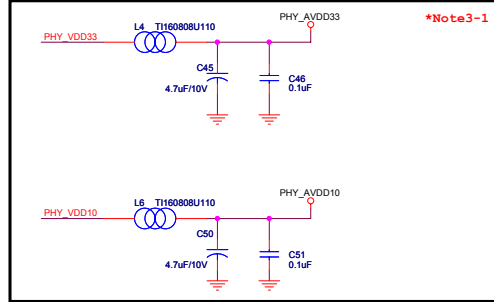
PHY Reset Circuit



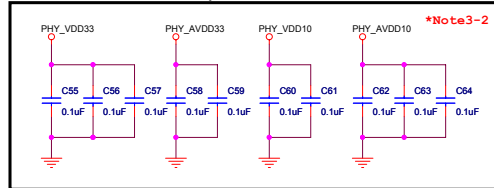
25MHz +/- 50ppm Crystal for Ethernet interface



PHY Analog power 3.3V/1.0V



PHY Power 3.3V and 1.0V By Pass



***Note3-1**
The C45, C46, C50 and C51 should be close to L4 and L6 as possible for reduce power noise.

***Note3-2**
Those 0.1uF by-pass capacitors should be as close to every power input pins as possible.

***Note3-3**
The R24 and C39 are reserved for EMI, please close to PHY as possible.

***Note3-4**
1.Enable On-chip Switch Regulator (Default)
Connect ENSWREG to PHY_VDD33 (i.e. Mount R36 and unmount R37)

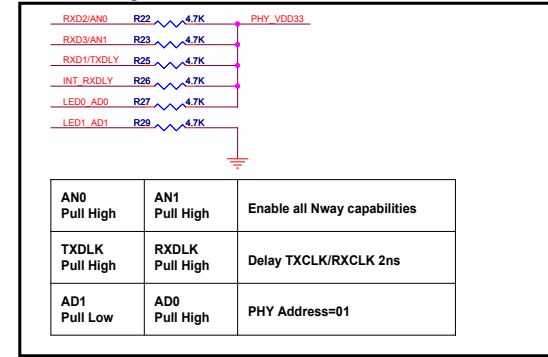
2.Disable On-chip Switch Regulator:
Connect ENSWREG to GND (i.e. Mount R37 and unmount R36)

***Note3-5**
The 3.3V power input VDDREG trace should be wider than 100mils (Keep floating while disabling on-chip switching regulator)
The capacitors C53 and C54 as close to the VDDREG pin (within 200mils) for good power efficiency.
C53 must be a ceramic (X5R) capacitor
C54 is recommended to be ceramic capacitor (Unmount L7, C53, C54 while disabling on-chip regulator)

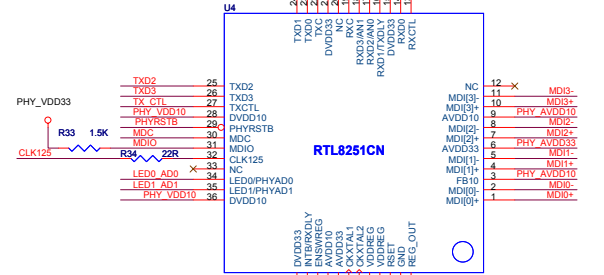
***Note3-6**
L5 (4.7uH) should be as close to RTL8251CN REG_OUT pin (within 200mils).
The 1.05V power output REG_OUT trace should be wider than 60 mils.
The C18 and C19 capacitors as close to L5 if possible. (Keep floating while disabling on-chip switching regulator)

***Note3-7**
The Ethernet LED circuit is a reference circuit while the PHY Address was set to 01h. (i.e. LED0_AD0 was pulled high and LED1_AD1 was pulled low)
Please refer to Realtek's GigaPHY reference circuit for more details if necessary.
The C52 and C65 are reserved for EMI please close to LED0_AD0 and LED1_AD1 pins.

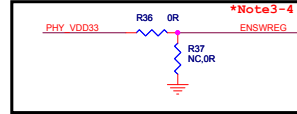
Hardware Configuration



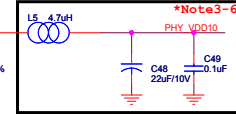
AN0 Pull High	AN1 Pull High	Enable all Nway capabilities
TXDLK Pull High	RXDLK Pull High	Delay TXCLK/RXCLK 2ns
AD1 Pull Low	AD0 Pull High	PHY Address=01



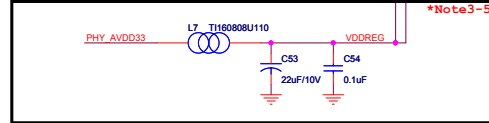
On-Chip Switching Regulator Circuit



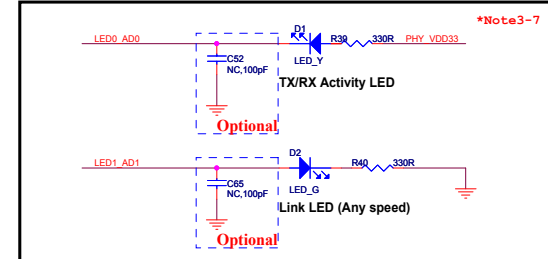
On-Chip Switching Regulator Circuit



PHY Regulator Power Input

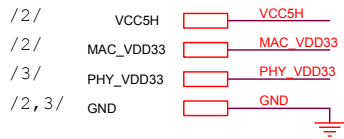


Ethernet LED Circuit

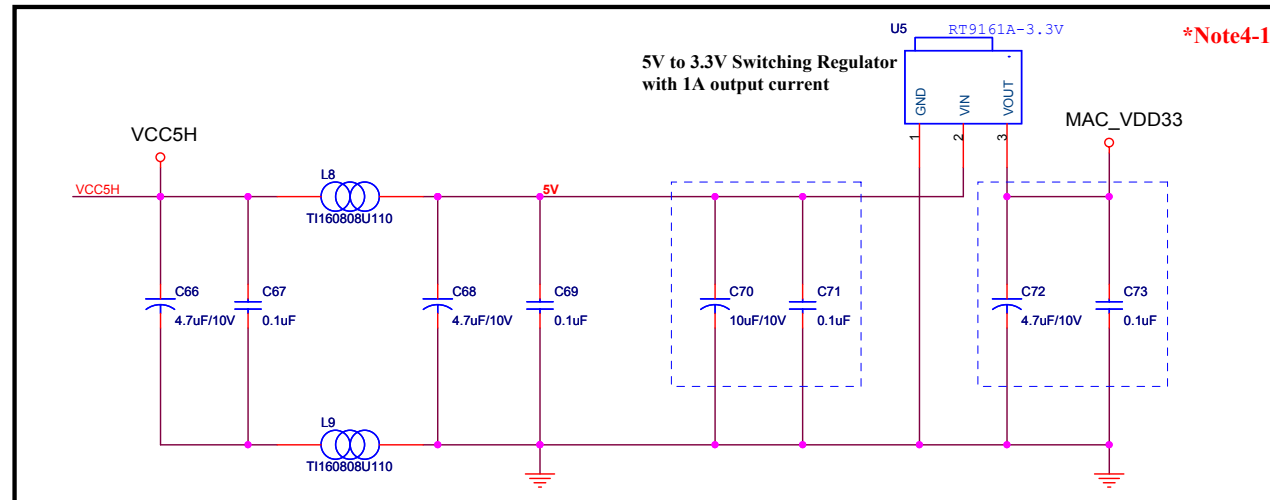


***Note:**
1.The RTL8251CN GigaPHY reference circuits are for customers' reference purpose.
Please contact Realtek's support guys to get the latest RTL8251CN reference schematic and Layout Guide before making your PCB board.

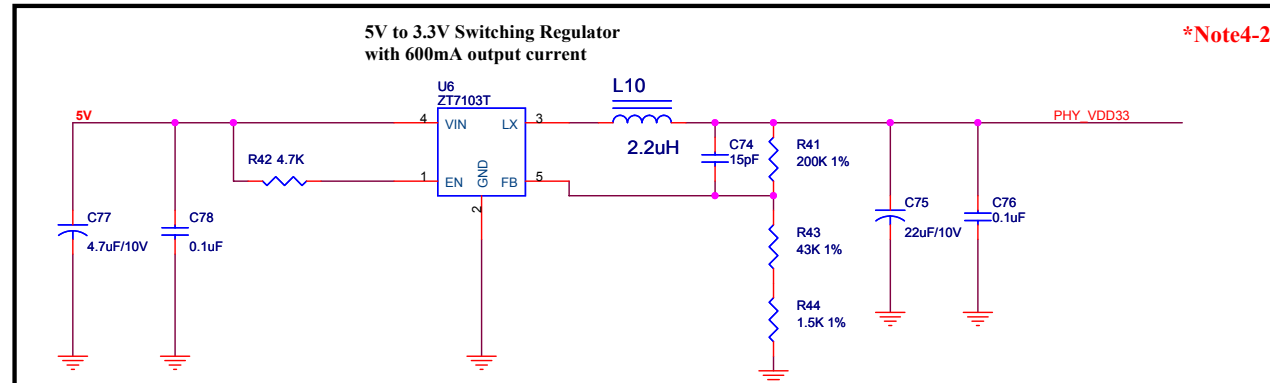
2.Please exactly follow up Realtek's RTL8251CN Layout Guide to layout RTL8251CN 3.3V to 1.05V On-chip Switching Regulator and Ethernet magnetic circuits; otherwise,the RTL8251CN might not work normally. Please refer to Realtek's layout guide for more details.



AX88180 Power Circuit



RTL8251CN Power Circuit



***Note4-1:**
The VCC5H should be kept the trace wider than 200mil.
The C66, C67, C68 and C69 as close to L8 for good power efficiency.

The 5V power trace as short as possible with Regulator input pin and kept the trace over than 100mils as possible.

The C70, C71, C72 and C73 as close to Regulator(U5) VIN/VOUT pins for good power efficiency and please kept the trace over than 50mils as possible.

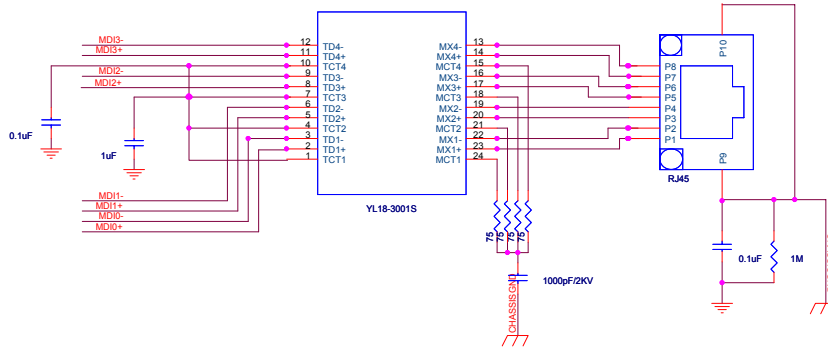
***Note4-2:**
The C77, C78 as close to Regulator(U6) VIN pin for good power regulation and kept the 5V trace wider than 100 mils.

The L10, C75 and C76 as close to U6's LX pin for good power switching.

***Note:**
The RTL8251CN GigaPHY power circuits and power consumption information are for customers' reference purpose.
Please contact Realtek's support guys to get more detailed information of RTL8251CN GigaPHY related power circuits and power consumption information.

ASIX ELECTRONIC CORPORATION		
Title		
Power Circuit		
Size	Document Number	Rev
B	AX88180+GigaPHY RTL8251CN Reference Schematic	1.00
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Reference Transformer Part
 No. list
 YL18-3001S
 YuTai Electronics Co.,LTD
 TEL:86-574-63620701,63621610
 http://www.yutai-elec.com
 EMAIL: nico_yu@yeah.net



Revision History

Revision	Date	Comment
V1.00	2010/07/22	Initial release.

AX88180+GigaPHY RTL8251CN Reference Schematic

AX88180 DEMO BOARD FOR S3C2440
 32 Bit Mode
 Little Endian

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Title Transformer+RJ45		
Size C	Document Number	Rev 1.00
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