

AX88772 Demo Board Reference Schematic Block

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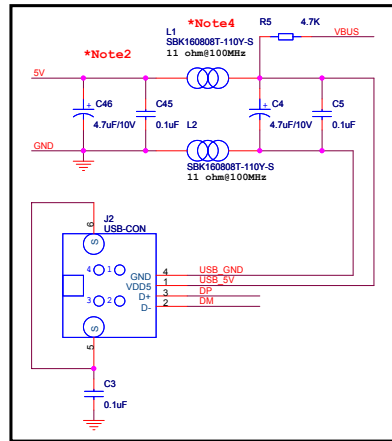
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Revision History

Note:

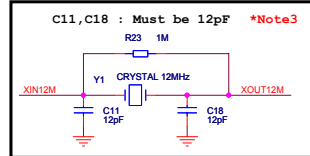
- 1. Please refer to AX88772 USB-to-LAN Application Design Note for more AX88772 PCB layout design notes.
- 2. Please contact ASIX Support (support@asix.com.tw) to get AX88772 EEPROM User Guide for more details about AX88772 EEPROM setting.
- 3. Please deliver us your AX88772 schematic and your AX88772 EEPROM data file for further review.

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Title AX88772 Application		
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USB Connector



12MHz +- 30ppm Crystal for USB interface



***Note1:**
AX88772 on-chip 3.3V to 2.5V regulator is a low dropout regulator (LDO), which requires some large external compensating capacitors on its input (pin #22) and output (pin #21) pins. The C1, C2, C28 and C51 capacitors are the compensating capacitors for the on-chip regulator.

***Note2:**
The L1, L2, C45, C46 and U5 should be as close as possible.

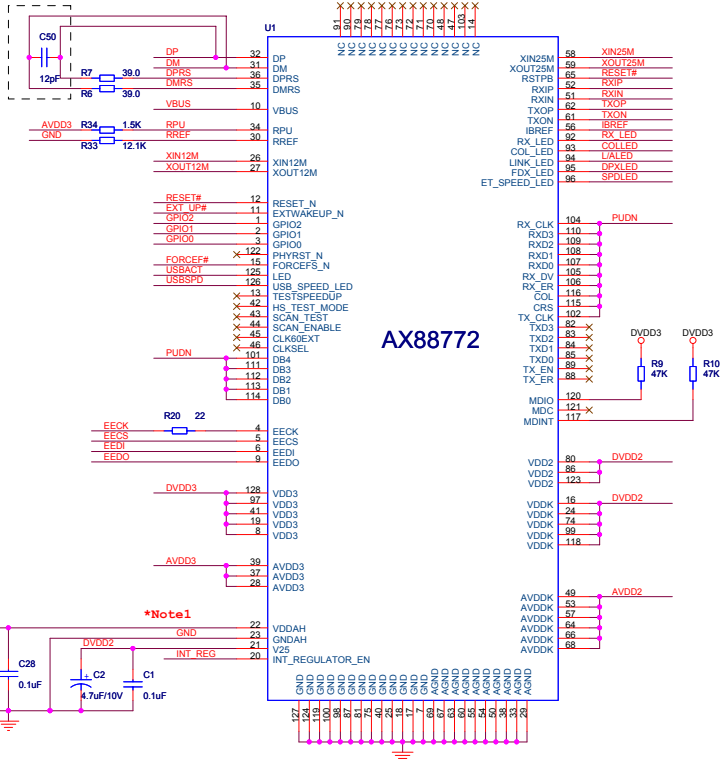
***Note3:**
The capacitor of 12MHz crystal clock MUST be 12pF. The following is the reason:
The AX88772 expects the ideal frequency range for the 12Mhz clock; this will give most margins for the internal PLL to generate a good 480Mhz clock, which is required by USB High Speed mode. That range is still within the USB 2.0 spec, which requires 480Mhz +/-500ppm accuracy.

Our extensive testing in the past showed higher capacitor value could put the 12Mhz out of above range, which sometimes can cause some problem during USB High Speed mode enumeration. For example, during the 100 times of repeatedly plug-and-unplug test, there may be 1 time that AX88772 may not be initialized properly. This is related to the bit error rate on USB bus in High Speed mode, which is higher if 12Mhz is out of above range. Therefore, we strongly suggest customers to use 12pF capacitor on 12MHz clock circuit for most stable operation of the chip.

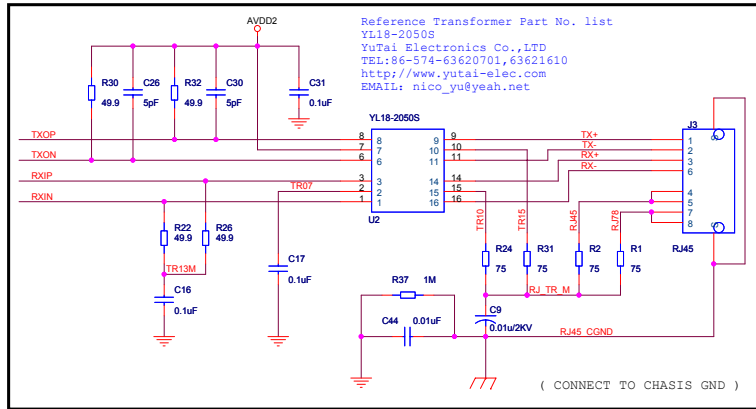
***Note4:**
The 5V power signals between the USB VBUS and the regulator 5V input should be isolated with a Ferrite Bead.

***Note5:**
The AX88772 EEPROM content includes some important hardware initialization data so it couldn't be removed on AX88772 application.

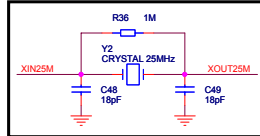
C50 : Option for docking



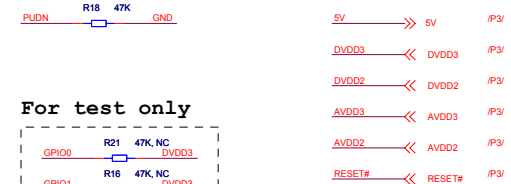
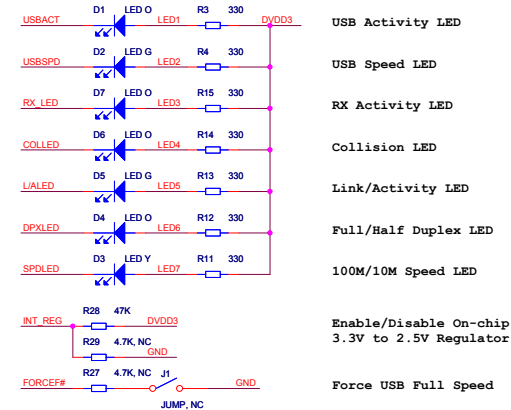
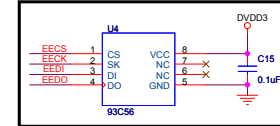
RJ-45 Connector + Transformer (Turns Ratio 1CT:1CT, without auto-MDIX)



25MHz +- 30ppm Crystal for Ethernet interface

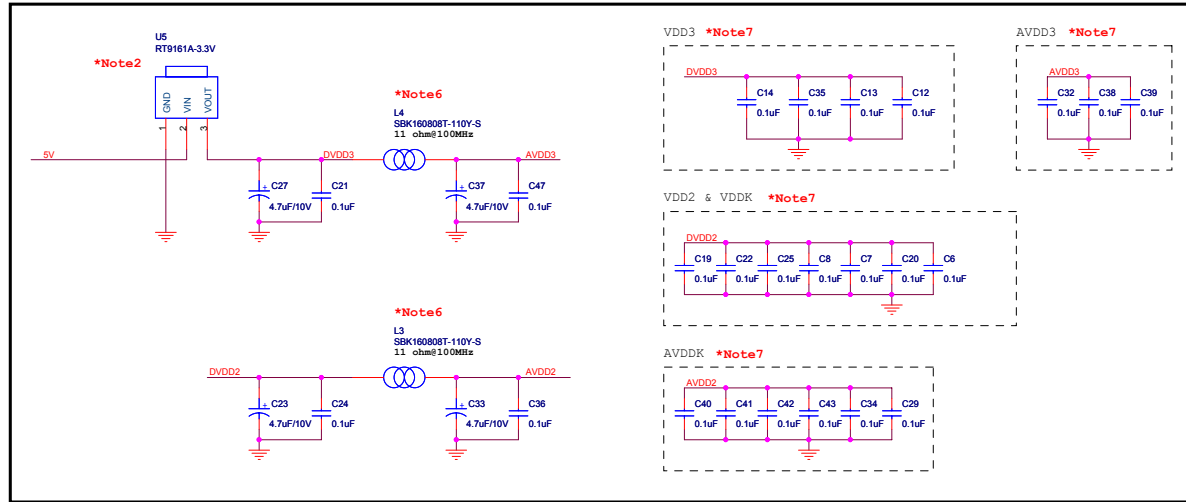
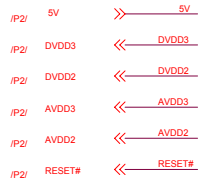


93C56 or 93C66 EEPROM ***Note5**

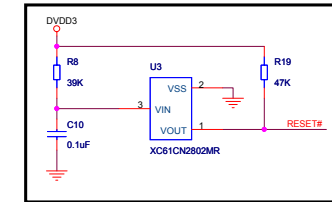


For test only

Power and by-pass capacitors *Note7



Reset Circuit



***Note2:**
The L1, L2, C45, C46 and U5 should be as close as possible.

***Note6:**
The analog powers and digital powers should be isolated with a Ferrite Bead.

***Note7:**
All power pins should be implemented with a by-pass capacitor, and the by-pass capacitor should be as close as the power pin.

V2.10 Version 2 Demo board Initial

V2.20

Add C50 for Docking

V2.21

Add description for C11 and C18

V2.22

Add C51 for Internal Regulator Input

Add description for L1, L2, C45, C46, U5

V2.23

Add description for R25, Normal R25 is NC, It's test only.

V2.24

Change pin 58 description from XOUT25M to XIN25M

Change pin 59 description from XIN25M to XOUT25M

V2.30

1. Re-arrange the whole schematic.

2. Add some notes to indicate the important information of this schematic.

V2.31 2009/05/18

1. Add some important note messages in Page 1.

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